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Design and Implementation of Cause-Based and Consequence-Based Control Circuits for Active Charge Balancing in CMOS Integrated Neural Stimulator

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"Do. Or do not. There is no try."
(Yoda)

Contents

Abstract

The treatment of neurological disorders and muscular disabilities is a challenging task. Functional electrical stimulation (FES) and functional neural stimulation (FNS), which excite nerves artificially by electrical charges, are impressive achievements for improving daily life quality of impaired patients. Two well-established examples are cardiac pacemakers and cochlear implants. In order to avoid charge accumulation at the electrode-tissue interface, which causes tissue lesion and electrode corrosion, charge balancing has become a major theme in safe electrical stimulation. Using biphasic current pulses, the main transferred charge is compensated by reversing the current direction within a stimulus. However, due to process variations in integrated circuits, mismatch in the biphasic waveform always occurs, hence, charge balancing as an additional safety aspect is indispensable. For reliability reasons, most certified medical devices are equipped with blocking capacitors or passive charge balancing, despite their large size, long settling time, and uncontrolled charge compensation. A promising approach towards small, fast, and well-controlled charge compensation is closed loop active charge balancing.

This thesis presents the author's research activities on the development of novel, CMOS integrated, low-power, high-voltage (HV) compatible, active charge balancing systems. Additionally, the thesis comprises the author's contribution to the development of a HV switch and an analog front-end neural stimulator that is used for all measurements to demonstrate the performance of the presented active charge balancing systems. Modern implantable stimulators have become highly specialized and adjustable to the challenges of diverse applications. Therefore, the developed, power-efficient and current-controlled stimulator is capable of supplying arbitrary programmable current pulse shapes and provides a HV compliance of up to 49 V. The stimulator is equipped with active charge balancing and passive charge balancing by a novel CMOS integrated HV switch. The main focus of this thesis lies on the development and implementation of the active charge balancing systems.

The first balancer presented provides long-term charge balancing, achieved by a cause-based proportional-integral (PI)-controlled Offset Compensation of the remaining electrode voltage. Here, the value of the remaining electrode voltage is monitored and serves as a measure for the stimuli mismatch. Thus, the amplitude of the cathodic current pulse of the presented stimulator front-end is adjusted accordingly. The system is very power-efficient and HV-robust. The balancer's monitoring amplifier provides an extraordinary small transconductance, which led to the first integrated PI controller for offset compensation in neural implants. Sev-

eral controller options are available to adapt to different electrode impedances, for which a detailed close loop stability analysis is presented.

Instantaneous autonomous balancing is realized by another, novel concept, the consequence-based Inter-Pulse Charge Control (IPCC). A class-B architecture is used to supply the compensation currents. In the implemented way, no additional references are required to define the safety window of the remaining electrode voltage. Thus, the IPCC features an autonomous charge removal at controlled compensation amplitudes after each stimulus. The compensation characteristic with continuous current supply makes the IPCC suitable as a complement to monophasic stimulators, replacing their missing biphasic counter pulse. Two implementations of the IPCC were realized. Both IPCC designs are power-efficient. However, while the first IPCC implementation is fixed to a 22 V supply, the enhanced design overcomes the technological HV limitations of the employed 0.35 µm CMOS process by using a quad-rail methodology and reaches a highly adaptive power supply compliance.

Each of the two complementary circuit solutions for cause-based and consequence-based charge compensation represents a sufficiently well performing control loop. However, providing the opportunity to achieve a better performance in charge balancing when being combined to the so called Twin-Track active charge balancer, and thus, accomplishing both: instantaneous and long-term balanced conditions. All charge balancers were characterized by simulations and verified by chip measurements via an equivalent electrical electrode model as well as in-vitro experiments.

Zusammenfassung

Die Funktionelle Elektrostimulation von Muskel- und Nervenfasern (FES und FNS) ermöglicht es, durch künstliche Anregung mittels elektrischer Ladung, neurologische und psychische Störungen oder Erkrankungen zu behandeln. FES und FNS tragen dabei erheblich zur Steigerung der Lebensqualität beeinträchtigter Patienten bei. Exemplarisch sind hier Herzschrittmacher und Cochlea-Implantate als gut bewährte und etablierte Elektrostimulatoren zu nennen. Das Prinzip des Ladungsausgleiches ist zum wesentlichen Bestandteil der sicheren Elektrostimulation geworden, um vor Gewebeschädigung und Elektrodenkorrosion, die aufgrund einer Ansammlung verbleibender Stimulationsladungen auftreten können, zu schützen. Zu diesem Zweck werden ladungsausgeglichene, biphasische Pulsstromquellen verwendet, welche den Großteil der übermittelten Ladung durch eine Richtungsänderung während der Stimulation kompensieren. Ob es nach einem Stimulationspuls zum vollständigen Ladungsausgleich kommt, hängt jedoch von der Diskrepanz der verwendeten Bauelemente der integrierten Schaltkreise ab. Jeglicher Unterschied in Amplitude und Dauer des Stimulationspulses führt zu einer Restladung über der Elektrode, weshalb eine Ladungsausgleichsschaltung als zusätzlicher Sicherheitsaspekt unabdingbar ist. Jedoch sind gängige zertifizierte Medizinprodukte meist lediglich mit Blockkapazitäten oder passiven Methoden zum Ladungsausgleich ausgestattet, welche einen großen Flächenbedarf, eine lange Einschwingzeit sowie einen unkontrollierten Ladungsausgleich aufweisen. Eine vielversprechende Alternative für eine flächeneffiziente, schnelle und kontrollierte Ladungskompensation bietet eine aktive Ladungsausgleichregelung.

Diese Arbeit präsentiert die Forschungsaktivitäten der Autorin im Bereich der Entwicklung von CMOS-integrierten, energieeffizienten und hochspannungskompatibler, aktiver Ladungsausgleichsmethoden und -schaltungen. Darüber hinaus umfasst diese Arbeit den Beitrag der Autorin zur Entwicklung eines Hochvolt (HV)-Schalters sowie des Analogteils eines CMOS-integrierten Nervenstimulators, welcher zu Messungen mit den hier vorgestellten, aktiven Ladungsausgleichsschaltungen verwendet wurde. Moderne implantierbare Stimulatoren sind hochspezialisiert und flexibel anpassbar an die Anforderungen verschiedenster Anwendungen. Der hier vorgestellte, energieeffiziente und stromgesteuerte Stimulator ist in der Lage, frei konfigurierbare Pulsformen zu generieren und dies bei einer Hochspannungsverträglichkeit von bis zu 49 V. Der Stimulator ist mit einem passiven Ladungsausgleich durch einen neuartigen CMOS-integrierten HV-Schalter und einer aktiven Ladungsausgleichsregelung ausgestattet. Der Schwerpunkt dieser Doktorarbeit liegt auf der Entwicklung und Implementierung der aktiven Ladungsausgleichsregelsysteme.

Das erste vorgestellte Ladungsausgleichssystem basiert auf einer PI-gesteuerten Offsetkompensation und wirkt der Ursache entgegen, die für die Entstehung einer Restspannung an den Elektroden verantwortlich ist. Hierfür wird die verbleibende Elektrodenspannung nach jedem Stimulationspuls integriert und gespeichert. Die Höhe der Restspannung gilt als Maß für die Stromquellendiskrepanz. Die Amplitudenhöhe des kathodischen Strompulses des vorgestellten Stimulator-Frontends wird entsprechend angepasst und somit ein langzeitiger Ladungsausgleich erreicht. Der Regler basiert auf einem Transimpedanzverstärker, dessen Besonderheit im außerordentlich geringen Transimpedanzwert liegt und somit den Grundstein zum ersten CMOS-integrierten PI-Regler zur Offsetkompensation in neuralen Implantaten legt. Diese Arbeit umfasst eine detaillierte Stabilitätsanalyse des hier vorgestellten Regelkreises zur Anpassung verschiedener Regleroptionen an unterschiedliche Elektrodenimpedanzen.

Ein sofortiger autonomer Ladungsausgleich nach jedem unausgeglichenen Stimulationspuls wird durch ein weiteres neuartiges Konzept erreicht: die konsequenzbasierte Zwischenpuls-Ladungsregelung. Auch hier werden verbleibende Ladungen über die Restspannung an den Elektroden überwacht. Sobald Sicherheitswerte der Elektrodenspannung überschritten werden, fließt ein Kompensationsstrom. Die Methode der IPCC nutzt eine Class-B-Architektur als Kompensationsstromquelle, was den Vorteil hat, dass keine zusätzlichen Bauteile notwendig sind, um das Sicherheitsfenster der verbleibenden Elektrodenspannung zu definieren. Auf diese Weise wird eine schnelle und kontinuierliche Ladungskompensation nach jedem Stimulationspuls erzielt. Die Kompensationscharakteristik ermöglicht, mit kontinuierlicher Stromzufuhr und kontrollierbarer maximaler Amplitude, zusätzlich den Gebrauch der IPCC als Ergänzung zu einem monophasischen Stimulator, indem es dessen fehlende Gegenpulse ersetzt. In dieser Arbeit wurden zwei Implementierungen der IPCC realisiert. Beide IPCC-Schaltungen sind energieeffizient und hochspannungskompatibel. Während jedoch die erste IPCC-Implementierung auf eine 22 V-Versorgung festgelegt ist, überwindet das verbesserte Design die technologisch bedingten HV-Limitierungen des verwendeten 0,35 µm-CMOS-Prozesses mithilfe einer Vier-Schienen-Methodik. Durch die neu erzielte, anpassungsfähige Hochspannungsverträglichkeit lässt sich die IPCC-Schaltung mit Stimulatoren unterschiedlicher Versorgungsspannungen kombinieren, ohne dabei ihre charakteristische Wirksamkeit zu verlieren.

Die beiden komplementären Ansätze zur ursachen- und konsequenzbasierten Ladungskompensation stellen jeweils einen eigenständigen, leistungsfähigen Regelkreis dar. In Kombination jedoch, als sogenanntes 'Twin-Track'-System, erhöht sich die Kompensationswirksamkeit, indem sowohl ein sofortiger als auch langfristiger ausgeglichener Ladungszustand erreicht wird. Alle Schaltungen wurden in einer 0,35 µm-HV-CMOS-Technologie entworfen und mit Simulationen auf Transistorebene charakterisiert und anschließend durch Chipmessungen über ein äquivalentes elektrisches Elektrodenmodell sowie In-Vitro-Messungen verifiziert.

1. Introduction

Electrical stimulation in the medical context is the use of electricity to treat a variety of physiological diseases and disorders. After a short excursion to the history of functional electrical stimulation, this chapter motivates the topic of charge balancing as an important safety aspect of electrical stimulation.

1.1. Functional Electrical Stimulation

The first record for functional electrical stimulation or neural stimulation (FES/FNS) as a therapy dates back to the year 46 BC, when Scribonius Largus used currents of electric rays from torpedo fishes for the treatment of gout and chronic headaches [1]. In 1791, experiments by Luigi Galvani demonstrated induced muscle contractions of a frog's leg by placing two different metals in series to the frog's leg and its spinal cord (Fig. 1.1). He named this effect 'animal electricity', assuming that the electricity is produced by the animal itself. Two years later Volta realized that the source of electricity was the bimetallic rod and that the frog's leg serves as electrical conductor [1].

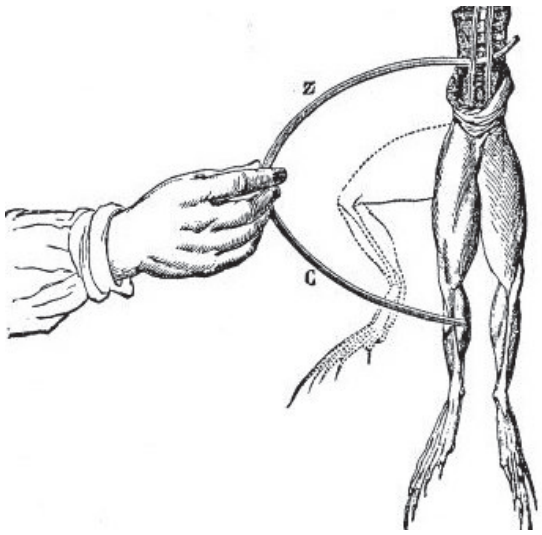


Figure 1.1.: Experiment of Luigi Galvani, showing muscle contractions of a frog's leg, induced by electrical discharge of a bimetallic rod (zinc (z), copper (c)). Taken from [1] (©1990, Springer).

Early in the 20th century, the nervous system was identified as the electrical conductor in animals and humans. It was demonstrated that propagation of action potentials can be triggered by applying a rapidly changing electric field near excitable tissue [2]. A first fully electrical stimulator was reported by Schmitt in 1932 [3]. Nowadays, FES is a well established treatment of a broad field of neurological or psychological diseases, in order to improve daily life quality of impaired patients by replacing physical functions previously lost or damaged. Beside cardiac pacemakers, impressive success is achieved with cochlear and retinal implants as hearing and visual prosthesis, peripheral nerve and muscle stimulators to overcome paralysis and aches, deep brain stimulation (DBS) to treat several types of neurological dysfunctions like Parkinson's disease, and vagus nerve stimulation (VNS) for blood pressure control [4–8].

1.2. Motivation

The motivation of this work is to find and elaborate different types of complementary metal-oxide semiconductors (CMOS) integrated circuits (IC) for active charge balancing in FES/FNS that are capable of reducing the hazards of electrical stimulation and facilitate safe chronic trials.

1.2.1. Importance of Charge Balancing

FES is a technique that excites nerves by inserting electrical charge into the body. However, this may lead to residual charges in the electrode-tissue phase boundary after stimulation. Using biphasic stimulus current pulses, the main transferred charges are compensated by reversing the current direction. Nevertheless, imperfections in the fabrication process of integrated circuits are unavoidable, leading to mismatch in the biphasic waveform. Accumulated charges do not only reduce the performance of subsequent stimulations, but worse, causes electrode corrosion and tissue lesion. Therefore, in order to avoid charge accumulation, in particular during long-term treatments, charge balancing (CB) has become an integral part of FES/FNS [9]. For reliability reasons, most certified medical devices are equipped with blocking capacitors or passive charge balancing systems, despite their disadvantage in size, long settling times, and uncontrolled charge compensation. A promising approach to small, fast, and well controlled charge compensation is active charge balancing. In addition to the general requirements of active implantable systems, such as low-power consumption and low-area demand, the diversity of applications necessitates a high adaptability and flexibility of the active charge balancing system. This implies for example configurable safety limits, output current limitations and adaptive supply rails with high-voltage (HV) compatibility. All these requirements are considered and incorporated in the presented charge balancing circuit solutions.

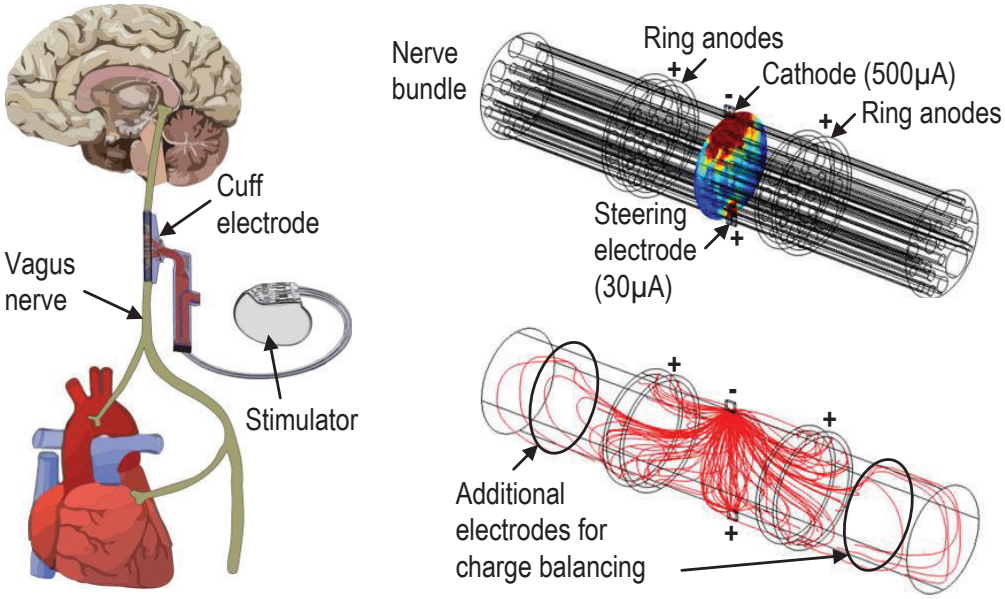


Figure 1.2.: Vagus nerve stimulation for blood pressure control by Baroloop (left) (reproduced and modified from [11] (©2009, Society for Neuroscience). Simulation of electrical field when using steering currents for an excitation of deeper nerve areas (right) (adapted from [12]). [13] (©2018, IEEE).

1.2.2. Further Benefits and Applications of Charge Balancing

Beside the need for CB as a safety feature, novel research issues raise the question of compensating remaining charges not only between two stimulation pulses, but in a precisely defined, small time frame. An application example [8] arises from one of our cooperation partners Dr. rer. nat. Plachta from Neuroloop GmbH, Germany. Their promising approach to overcome chronic hypertension is selective VNS by the system BaroLoop [7]. At the event of an increased blood pressure, e.g. caused by altered stiffness of the arterial wall, the strength of the afferent nervous signals is reduced. The solution is to override the vagal signal with the help of artificial electrical stimulation. However, the transfer of blood pressure information to the brain is only one of the vagus nerve's functions. The inadvertent stimulation of non-baroreceptive fibers may cause severe side effects like bradycardia and bradypnea [8]. Therefore, BaroLoop aims to localize the relevant fibers and extract blood pressure information by tripolar recording [10] via a cuff electrode [8], which is wrapped around the vagus nerve as illustrated in Fig. 1.2 left. The localized electrode tripole is then used for selective stimulation.

The ongoing fundamental research idea of this group is to equip the stimulator setup with the capability to influence the direction of action potential (AP) propagation via steering currents. These steering currents, originating at neighboring stimulation sites, are used to either fine tune the applied current for an improved efficacy or to block the spreading of activity in unwanted directions using anodal blocks.

The principle of steering currents with 30 µA versus 500 µA stimulation currents, is illustrated in Fig. 1.2. The steering electrode is located at the opposing stimulation site in order to focus the electrical field deeper within the nerve. The distribution of the electrical field lines, as presented in the simulation results in Fig. 1.2 (right, bottom), expand even beyond the anodal rings, thus, leading to charge redistribution at neighboring sites. Therefore, it is of interest to place additional autonomous and stand-alone CB systems in some distance apart from the actual stimulation site to block the spreading of activity in unwanted directions.

Additionally, in case of inhibitory prestimulation at neighboring sites, the investigated stimulation electrode might be affected by cross-talk effects, which reduce the efficacy of the desired stimulus. Therefore, CB timed in between the inhibitory and excitatory stimulation pulses can compensate for charge imbalances caused by adjacent electrodes. It thus assists the stimulation site to regain the resting potential rapidly, resulting in an increased treatment efficacy and potentially decreased side effects. In applications with monophasic steering currents, where preprogrammed biphasic counter pulses for CB are not suitable, a charge balancer that is capable of generating counter pulses autonomously, with self-adaptive timing, is desirable.

Another application scenario with even higher challenges to the neural interface is the recording of an AP resulting from an artificial stimulus itself [14]. Such analyses will provide insights into the effects of artificial neural stimulation and the processes of neuro-modulation. For instance, in a design with DC-blocking capacitors large equalization currents hinder spinal cord potential measurement attempts [14]. For this reason, controlled and fast charge compensation is desired to bring back the electrodes that monitor the evoked AP to the body's resting potential. Since the AP signal amplitude is short and small, typically in the range of micro-volts, digital signal interference and artifacts at the sensing electrode should be avoided. Therefore, active CB in from of an analog background operation is desired and suitable to improve the signal quality during experiments with simultaneous measurement and stimulation.

In summary, CB may offer a basis for further investigations of novel research issues such as controlling the direction of AP propagation or improving the quality of simultaneous measurement and stimulation. The mentioned application examples demand a close loop balancer for an analog background operation as well as a self-adaptive balancer with automatic counter pulse generation that can be used as a stand-alone implementation. The CB solutions of this work may thus help to answer current questions and define the future roadmap for research on implantable neural interfaces.

1.3. Thesis Organization

This thesis is divided into nine chapters, which are organized as follows:

Chapter 1: *Introduction.* This chapter introduces electrical stimulation. Further, the idea and importance of charge balancing, which is the focus of the thesis, is motivated.

Chapter 2: *Fundamentals.* Although action potentials are generated physiologically, the excitation of nerves can be artificially triggered by injecting electrical charges into excitable tissue. A fundamental knowledge about anatomy and physiological excitation of nerves is required to understand how nerves can be excited technically. An insight about various charge delivery strategies, including stimulation parameters and waveforms, different electrodes and their configurations to achieve good selectivity is given. During stimulation a current transfer at the electrode-tissue interface from electron conduction in the metal to ion conduction in the electrolyte takes place. Having a closer look at this phase boundary provides a better understanding of the charge transfer processes, that lead to the equivalent electrical model of the electrode-tissue interface. The model allows to relate accumulated remaining charges to a remaining electrode voltage that is controlled and kept within a predefined safety limit by charge balancing. Thus, this chapter emphasizes the significance of charge balancing for safe electrical stimulation, since it reduces the risk of tissue damage and electrode dissolution, which might arise after unbalanced stimulation pulses.

Chapter 3: *State-of-the-Art Charge Balancing.* Beside the attempt to decouple DC voltages at the electrode by blocking capacitors, closed loop charge balancing systems are a promising alternative for small, fast, and controlled charge compensation. For a better overview, state-of-the-art charge balancers are classified into compensation methods that differ in their mode of action, introduced as consequence-based and cause-based charge compensation.

Chapter 4: *Overall System Description and Stimulator Front-End.* This chapter shows the conceptual configuration of the stimulator front-end with the proposed charge balancing circuits, which interface at the electrode. Due to the HV stimulation environment, all circuits and components must be HV compliant. Therefore, a general quad-rail methodology is presented that allows for HV compatible, power-efficient, and supply rail independent circuit designs. The section about the stimulator front-end starts with the investigation of the most beneficial current mirror topology as the basic concept of the current source design for a flexible current-controlled stimulation. The discussion is followed by the circuit implementation and measurement results with the focus on HV robustness, low-power consumption and the ability of controlled arbitrary waveform generation. Subsequently, the design and implementation of the HV compliant switch is introduced. The latter is an important interface component that separates the active charge balancing circuits from the stimulator circuitry. Additionally, the same switch architecture is

implemented for passive charge balancing, shorting the electrode via its switched on-resistance.

Chapter 5: *The PI-Controlled Offset Compensation* is the cause-based active charge balancing system. To monitor the low-frequency bio signals a large time constant in the milli-second range is necessary. Therefore, the PI controller was realized by a very low transimpedance amplifier, which is the heart of the circuit, and an on-chip capacitance. The design architecture and measured characteristics are presented, followed by the stability analysis of the PI-control loop. Finally, the PI-controlled Offset Compensation is compared to state-of-the-art charge balancers.

Chapter 6: *The Inter-Pulse Charge Control* is the consequence-based charge balancing circuit. A HV compliant amplifier monitors remaining charges and steers an advanced HV class-B push-pull stage, representing the compensating current source. Two circuit designs were implemented, both based on this novel and innovative compensation concept. The circuit designs and measurement results are presented and compared to each other, as well as to the state of the art.

Chapter 7: *The Twin-Track Charge Balancer* is the combination of the PI-controlled Offset Compensation and the Inter-Pulse Charge Control. The advantages of a Twin-Track charge balancer are explained and demonstrated by system measurements.

Chapter 8: *Conclusion and Outlook.* The last chapter concludes this work by highlighting the main achievements. A short outlook to future work is supplemented.

2. Fundamentals

Modern implantable stimulators have become highly specialized and adjustable to the challenges of diverse applications. In safe electrical stimulation charge balancing is a major concern, since it controls the reversion and compensation of remaining injected charges to regain the tissue's charge balanced equilibrium. Thus, reducing the risk of irreversible reactions that lead to electrode dissolution, pH change and tissue damage. This chapter[1] explains the physiological and technical nerve excitation. It gives an insight about various charge delivery strategies, stimulation waveforms, and electrode configurations to achieve good selectivity. Further, this chapter provides a closer look at the phase boundary to understand the charge transfer processes and derive an equivalent electrical model of the electrode-tissue interface. The model allows to relate accumulated charges to a remaining electrode voltage that is controlled and kept within a predefined safety limit by charge balancing.

2.1. Biomedical Background

The nervous system (NS) contains all neurons (nerve cells) and glia cells and can be distinguished into the central NS (CNS) and the peripheral NS (PNS). The CNS includes the brain and spinal cord, whereas the PNS is a collective term, representing the remaining parts of the NS, such as the nerves contacting muscles and organs. According to its body functions, the NS can be divided into the autonomic NS (Symphaticus and Parasymphaticus), which regulates organ functions and can hardly be influenced by will, and the somatic NS, which controls muscle functions and is influenced by will. Neurons that carry signals from sensory receptors in the PNS to the CNS are called afferent neurons. Efferent neurons, also known as motor neurons, carry signals from the CNS to the muscles or glands of the PNS [1].

2.1.1. Anatomy of Nerves

In Fig. 2.1(a) the anatomy of a nerve is shown, consisting of multiple fascicles and blood vessels wrapped in a layer of connective tissue. Each fascicle is an enclosed bundle of nerve fibers. A myelinated fiber is the axon of a single neuron, covered by

[1]The fundamentals summarized in this chapter have been partially published in a similar way in [15] by the author of this thesis.

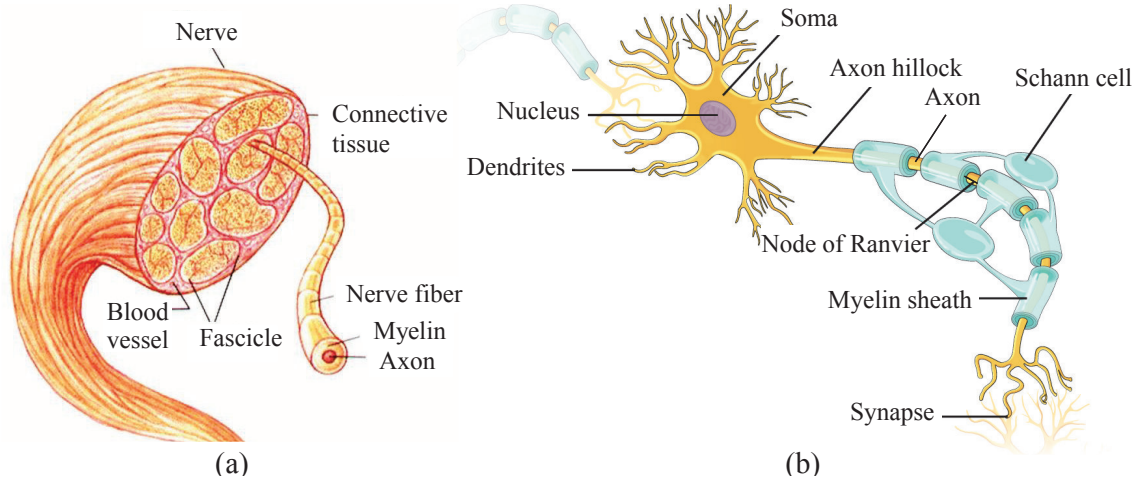


Figure 2.1.: Anatomy of (a) the nerve, consisting of multiple fascicles and blood vessels wrapped in a layer of connective tissue (adapted from [16]), and (b) of the myelinated neuron (adapted from [17]).

a layer of insulation called myelin sheath. A neuron, as illustrated in Fig. 2.1(b), consists of four major components: the cell body (soma with nucleus), the receptor zones (dendrites), the conductor (axon) and its terminals (synapse). The myelin sheath of the axon is an outgrowth of the Schwann cell. It is absent at the so called nodes of Ranvier, at which transmembrane ionic transfer occurs, allowing for saltatory signal conduction. The axon carries the electrical signals from the soma to the target sites such as muscles, glands, or other neurons (dentrites). The synapses are separated from the soma of their target sites, by narrow gaps. Electrical signals that arrive at the synapse are translated into chemical signals by the release of transmitters. These transmitters travel across the synaptic gap, thereby altering the membrane potential of the target site and resulting to the post-synaptic-potential (PSP). If a sufficient excitatory PSP reaches the axon hillock of a neuron, the electrical signal in form of an actively sustained action potential (AP) is triggered.

The medium inside and outside the neuron consists of water and ions. The cell membrane serves as an insulator and diffusion barrier for ions, but has certain semipermeable characteristics that allow specific ionic interchanges, see Fig. 2.2. The ionic channels in the membrane can vary their permeability in response to the transmembrane potential, allowing ions to move across the membrane down a concentration gradient. Further, ion pumps actively push ions across the membrane to establish concentration gradients across the membrane. Concentration gradients of ions across the cell membrane can be described as electrical and chemical forces. The ambition for charge equalization counteracts the ambition for concentration equalization (diffusion). In an equilibrium stage potassium (K^+) is highly concentrated in the intracellular fluid (Cytosol) and is at low concentration in the extracellular, whereas sodium (Na^+) and chloride (Cl^-) are highly concentrated in the extracellular fluid and at low concentration in the intracellular. In electrochemical equilibrium neurons

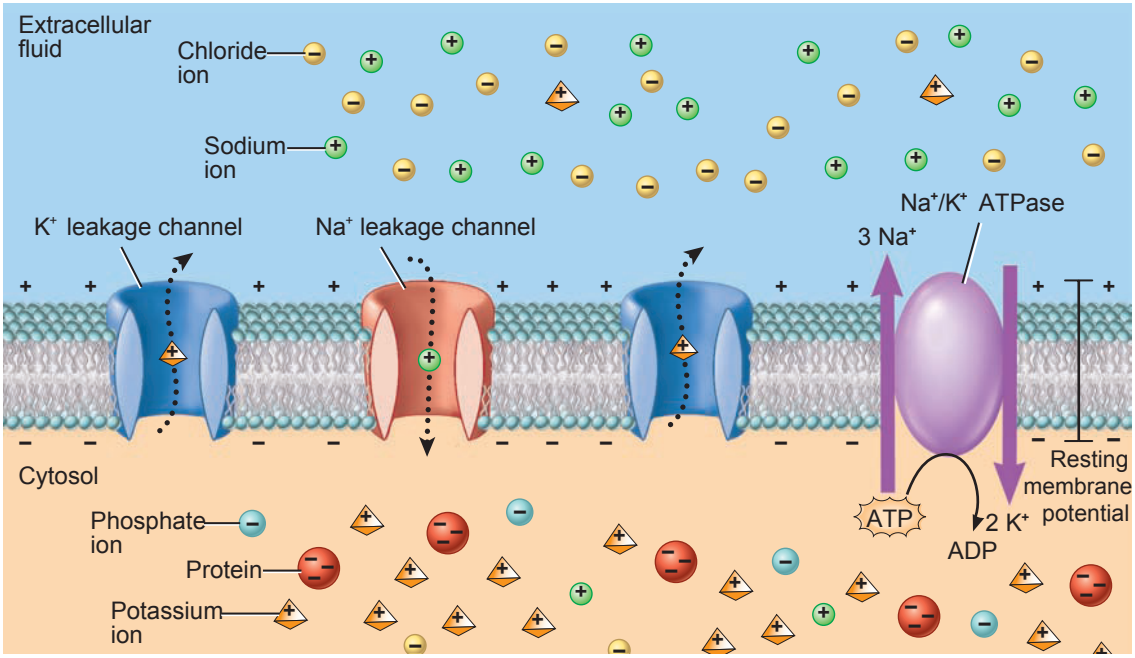


Figure 2.2.: Ionic concentration at the membrane at rest and the ionic current through the ion channels. Reproduced from [21] (©2009, John Wiley and Sons).

maintain a resting membrane potential typically around −60 mV to −90 mV, with the interior being negative with respect to the exterior of the cell [18–20].

2.1.2. Physiological Nerve Excitation

An AP is generated once the resting membrane potential at the axon hillock is increased beyond a threshold value by roughly 15 mV. Once the threshold is reached, the transition between resting and excited condition of the membrane occurs rather abruptly (few ms) and in a characteristic manner, as illustrated in Fig. 2.3 [18]. The first phase of the AP called depolarization, is a steep rise in potential from the resting potential to a positive potential of around 20 mV to 40 mV, under the condition that the excitation exceeds the threshold value. During repolarization, the second phase, the potential drops abruptly below the resting potential leading to the third phase, the hyperpolarization. During the absolute refractory period, a second AP cannot be initiated, independent of the strength of the applied stimulus. This interval is immediately followed by the relative refractory period in which initiation of a second AP is inhibited but not impossible. In this way refractoriness prevents backward propagation after an AP has occurred [22].

The change in charge ratio during an AP is accomplished by a delayed opening of the voltage-gated ion channels (Fig. 2.3). These channels are shut for a membrane potential that is close to the resting potential. Depolarization above threshold provokes the Na^+ channels to rapidly open, allowing an inward flow of Na^+ ions, which

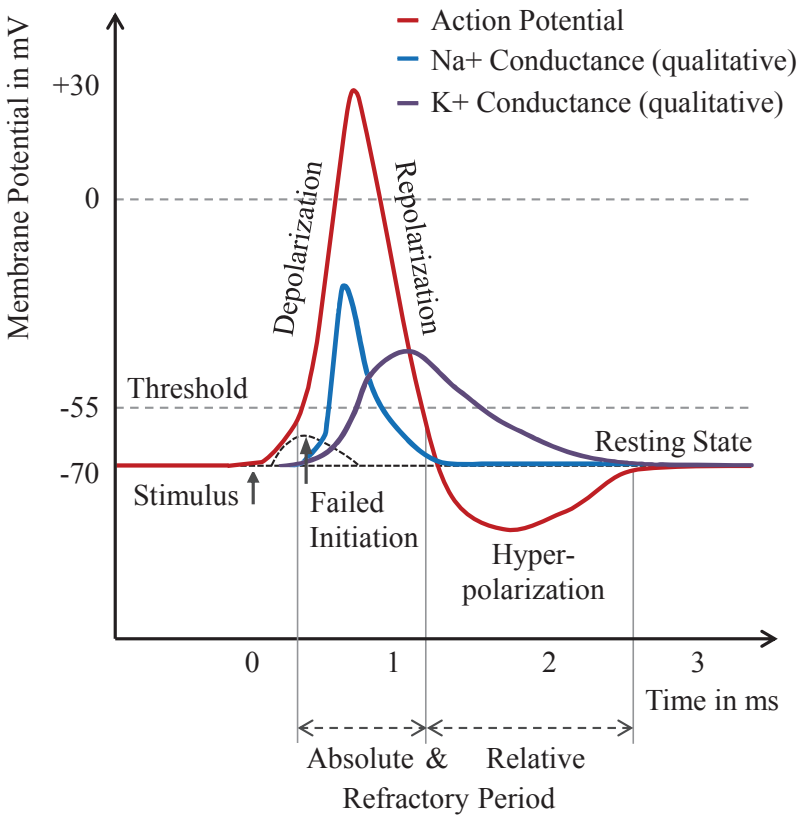


Figure 2.3.: The phases of an action potential and the corresponding conductance of the two major ion channels. Reproduced and modified from [23].

produces a further rise in membrane potential (depolarization). By reversion of the membrane potential, the Na^+ channels close and the permeability for Na^+ decreases again. Almost simultaneously with the opening of the Na^+ channels the K^+ channels slowly start to open. As these channels exhibit inertia, the permeability of K^+ ions is still increasing, while the Na^+ channels are already closed, thus, returning the electrochemical gradient to the resting state (repolarization). The inert behavior of K^+ channels cause additional K^+ currents after the resting potential is reached, leading to hyperpolarization. After an AP has occurred the ionic distribution of the resting potential is reestablished by the Na-K-Pump under the consumption of metabolic energy Adenosine Triphosphate (ATP) [22].

In unmyelinated nerve fibers, voltage-gated ion channels are located all over the membrane. Thus each membrane area, along the full length of the axon, needs to be excited consecutively for AP propagation. The AP spreads along the axon, depolarizing adjacent region of the axon. This type of propagation depends on a number of factors, for example the cross-sectional width of the axon. For nerve fibers of class C according to Erlanger/Gasser, the propagation velocity is typically around 1 m/s at a mean fiber diameter of 1 µm [24]. Although increasing the diameter leads to an increased velocity, unmyelinated conduction is rather slow and not suited for

higher speed requirements. A faster and more efficient conduction is promoted by myelinated fibers. Myelin sheaths of up to 2 mm long sections are wrapped around the axon, efficiently insulating it [25]. Voltage-gated ion channels are only located at the nodes of Ranvier. The AP propagates along the myelinated axon by jumping from one node of Ranvier to the next (saltatory conduction). It therefore propagates faster along the axon as it would in the absence of myelin. The conduction velocity is increased without the need to increase the axon's diameter. For nerve fibers of class A according to Erlanger/Gasser, the propagation velocity can go up to 120 m/s at a mean fiber diameter of around 15 µm [24]. An important property of action potential propagation is the all-or-none law, which holds for both conduction types. It reveals that if the stimulus is above threshold, the nerve will give a complete response. Otherwise no response at all will be generated. An AP is then propagating without decreasing its amplitude over the entire length of the nerve fiber. The depolarized regions are the stimulus for adjacent regions [22].

2.2. Technical Nerve Excitation

Electrical stimulation of nerves is the technically triggered excitation of a neuron by artificially depolarizing the axon's membrane. Technical systems interface nerves via electrodes, which are placed in direct contact with the excitable tissue. During stimulation a current transfer from electron conduction in the solid state of the electrical circuit to ion conduction in the fluid state of the electrolyte takes place, leading to a potential difference between the extracellular and intracellular fluid of the neuron at the electrode site. In Fig. 2.4 the effect on the membrane's potential of an axon is shown for a positively charged electrode during an anodic stimulus, and a negatively charged electrode during a cathodic stimulus. A positively charged electrode leads to hyperpolarization, whereas the negatively charged electrode triggers APs at adjacent nodes of Ranvier in both directions, presupposed that the potential difference exceeds the threshold value.

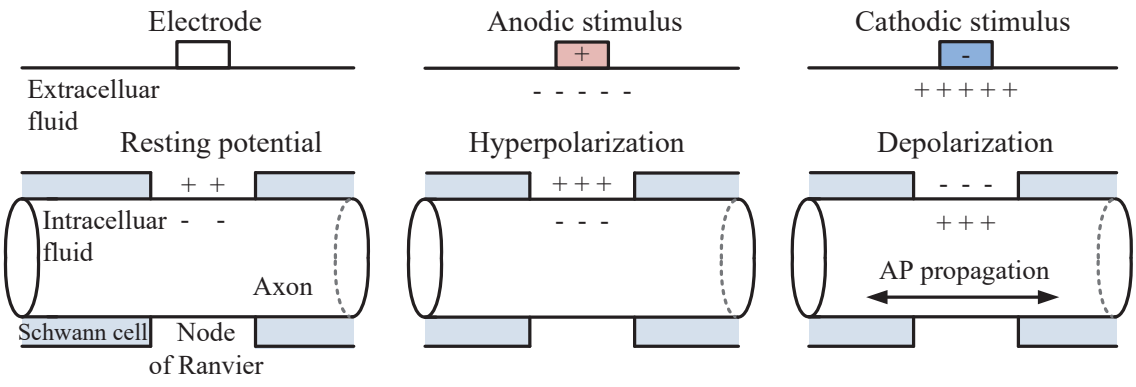


Figure 2.4.: The effect of electrode polarization during technical nerve excitation.

2.2.1. Charge Delivery Strategies

There are basically three different methods to polarize the electrode: voltage, charge, and current mode stimulation [6]. They are physically linked but describe different approaches for charge delivery, i.e. controlled by a voltage source, capacitive discharge, or a current source. Voltage controlled stimulation suggests itself, since the electrical excitation is dependent on the voltage applied across the neuron's membrane. However, it is the charge that has to be controlled, since the metal-electrolyte interface is characterized by a maximum allowed charge that can be transferred from the electrode into the biological tissue. Additionally, taking into account that the load impedance varies over time, the injected charge differs when using voltage-controlled stimulators, which is why they are rarely used in modern implantable systems [4, 5]. Using charge-controlled stimulation via capacitive discharge, the stimulation charge is accurately controlled [6, 26–28]. However, in case of high load capacitances, large discharge capacitors are required for sufficient charge delivery, which is a disadvantage for implantable micro systems. Furthermore, the waveform of the applied charge is predefined by the discharge characteristic and offers little flexibility. Current-controlled stimulation, in which pulse width t_w and stimulus current amplitude I_Stim is controlled regardless of impedance variations, are most commonly used [4, 5, 29], as charge and current are directly linked by

$$Q = \int_0^{t_\mathrm{w}} i(t)dt = I_\mathrm{Stim} \cdot t_\mathrm{w}\,, \tag{2.1}$$

when rectangular stimulation is applied. Nevertheless, when using current-controlled stimulation it has to be considered that for high load impedances, high voltages are required to accommodate a certain level of current, requiring HV CMOS processes for application specific IC (ASIC) development. Therefore, beside current-controlled stimulators at low-voltage (LV) supplies with a maximum compliance of 3 V to 5 V [6, 30–32], HV compliant stimulators in the range of 20 V to 36 V have been published in [4, 5, 33–36]. For each application, the relationship between amplitude and pulse width for a successful stimulation can be experimentally derived by the strength-duration curve [2]. A strength-duration curve is exemplarily shown in Fig. 2.5. The amplitude of the threshold current I_th, required to rise the membrane potential above threshold, decreases with increasing pulse width t_w until a minimum current amplitude, the rheobase current I_rh, is reached. The minimum t_w, that is needed for nerve excitation, with a current amplitude of twice I_rh, is called chronaxie time t_c. Both values are useful to describe the electro sensitivity of the target tissue [2, 37].

Different current waveform shapes like square, sinusoidal, ramp, or exponential are possible for successful stimulation and their efficiency and effect of parameters are analyzed by [38, 39]. However, the shape of waveform is irrelevant for the success of charge balancing. Since the focus lies on charge balancing, only monophasic and biphasic rectangular pulses, as shown in Fig. 2.6, are considered in this work. Monophasic stimulation consists of a negative (cathodic) stimulation pulse, illustrated in Fig. 2.6(a), that depolarizes the nerve, and thereby, evokes the desired

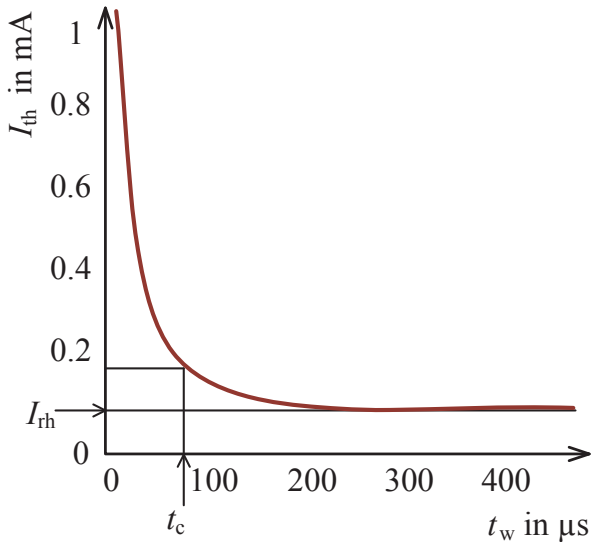


Figure 2.5.: Strength-duration curve. Reproduced from [2].

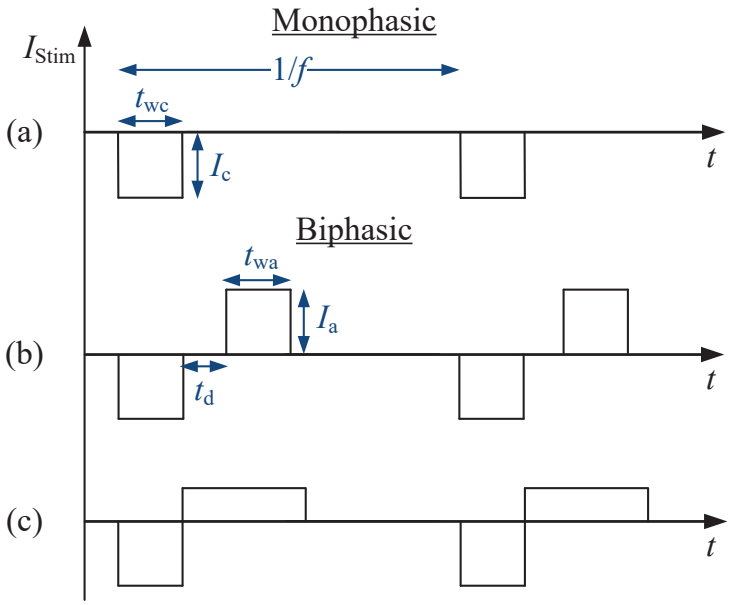


Figure 2.6.: Rectangular stimulation waveforms, (a) monophasic stimulus, (b) symmetric rectangular biphasic waveform with cathodic-first current and pulse delay, and (c) asymmetric biphasic waveform with cathodic-first current.

physiological effect. The characteristic parameters are cathodic amplitude I_c, cathodic pulse width t_{wc}, and stimulation frequency f. The more commonly used biphasic stimulation waveform, illustrated in Fig. 2.6(b) and (c), consists of a cathodic stimulating phase and an anodic counter phase, reversing the electrochemical reactions by a pulse of opposite sign [40]. Beside the cathodic parameters and stim-

ulation frequency, the biphasic waveform is characterized by anodic amplitude I_a, pulse width t_{wa}, as well as a possible delay time t_d between the two phases. Typical values for FES given by [41] are current amplitudes $I_{a,c}$ of 1 mA, pulse widths t_w of up to 500 µs, and stimulation frequency f of 10 Hz to 30 Hz. A perfectly balanced stimulus provides equal amount of positive and negative charges, however, $I_{a,c}$ and $t_{wa,wc}$ can be chosen identical (Fig. 2.6(b)), or asymmetric (Fig. 2.6(c)). Biphasic waveforms with cathodic-first current are usually favored, since the anodic pulse hyperpolarizes the nerve and elevates the excitation threshold [42].

2.2.2. Electrodes

For chronic implantation, long term biostability of the electrodes with minimal corrosion must be provided for several decades. Commonly used materials for stimulation electrode contacts are non-noble metals like stainless steel 316 or nickel-cobalt alloys, as well as noble metals, such as platinum and iridium oxide. Noble metals are preferred for electrical stimulation due to their smaller corrosion rates. However, corrosion still takes place during electrical stimulation and can be observed by weight loss, dissolution of metal ions and deposition of the ions in the surrounding tissue. Corrosion does not only result in deterioration and destruction of the electrode material, but also in tissue damage [43]. Thin film electrodes are manufactured by means of microsystem technologies and clean room processes. Different designs of multichannel electrode arrays offer a preselection of the working electrode, to stimulate a certain envisioned site of the nerve. The shaft array, shown in Fig. 2.7, belongs to a kind of intraneural electrodes, also referred to as intrafascicular electrodes that are placed directly inside the nerve by penetrating the tissue. The close proximity to the target site allows good stimulation selectivity. However, penetrating the nerve during implantation can lead to significant nerve damage.

The spiral multichannel cuff electrode, shown in Fig. 2.8, represents an extraneural electrode array that interfaces the nerve by surrounding its surface without penetrating nervous tissue [2]. The anatomical structure of the nerve remains intact during and after implantation. Compared to intraneural electrode concepts, the advantage of less invasiveness and self-sizing properties is accompanied by some disadvantages, such as an increased current threshold to excite nerve fibers. The high number of electrode sites on the inner perimeter of the cuff allows selective stimulation of different parts of the nerve on the fascicular level. However, the ability to selectively stimulate different nerve fibers is limited, since only bundles of fibers can be stimulated simultaneously. A cuff electrode, like the one shown in Fig. 2.8, provided by neuroloop GmbH, Freiburg, Germany, is used for system verification in this thesis. The cuff is manufactured as a planar sheet, then tempered to roll and shape it into a three-dimensional structure. For the thin film metallization layer, 300 nm platinum is sputtered and coated with 1000 nm iridium oxide. Polyimide is used as substrate and insulation material. The cuff features 24 working electrodes, arranged in three rows of eight electrodes each, and four adjacent outer ring electrodes, all facing

inside the cuff. Two electrodes facing outside are provided as reference electrodes. The cuff's total length is 20 mm and the inner diameter is 0.8 mm [7, 8, 44].

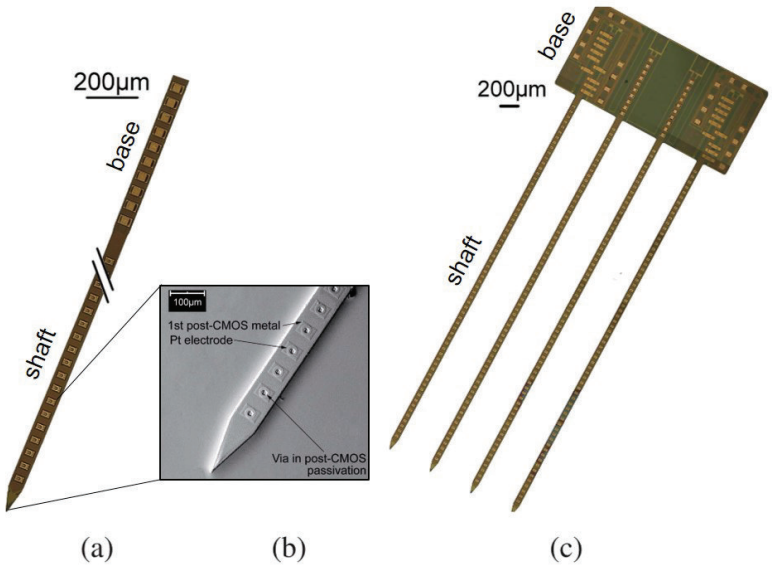


Figure 2.7.: Micrograph of neural electrode shaft arrays. (a) Slim shaft. (b) Scanning electron microscopy micrograph of the tip section. (c) Combination of multiple shafts into a comb structure. Modified from [45] (©2018, IEEE).

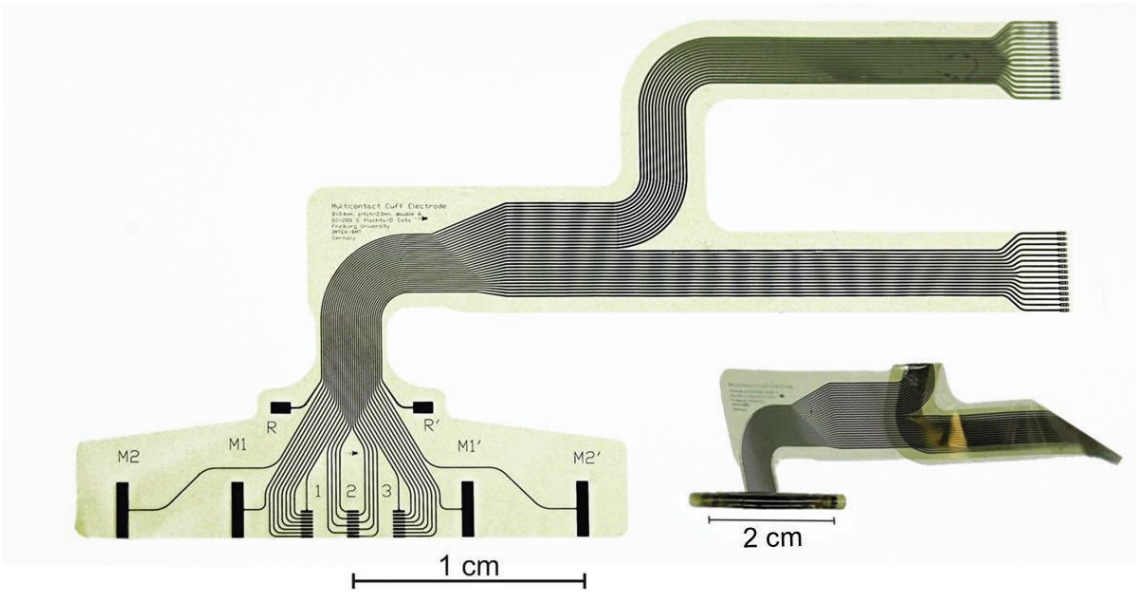


Figure 2.8.: Photograph of the polyimide thin film cuff electrode. Large image: after micromachining with eight electrodes arranged in tripoles in the middle (1, 2, 3), four outer ring electrodes (M1, M1', M2, M2'), and two reference electrodes (R, R'). Small image: spiral cuff in its wrapped condition. Modified from [8, 44].

2.2.3. Selectivity

The selectivity of a target tissue or selected nerve fiber can be improved by the choice of an appropriate electrode configuration and stimulation technique. At least two electrodes are necessary to provide a current flow for electrical stimulation, the working electrode and a counter electrode. In case of monopolar stimulation (Fig. 2.9(a)), the electrons arrive on the working electrode with a relatively small surface area. The counter electrode has a larger surface area and can be located within quite a distance. It is basically the ground electrode, which exhibits the body's quiescent potential. The current is focused near the electrode and tends to enter the insulation material of the electrode array at its ends in a uniform way. Bipolar stimulation (Fig. 2.9(b)) is similar to monopolar stimulation, but the counter electrode is located on the electrode array and is of opposing polarity. The position and size of the counter electrode defines the shape of the electrical field. Another possible electrode configuration is tripolar configuration (Fig. 2.9(c)), where two adjacent electrodes are used as counter electrodes with opposing polarity [34, 39]. The current will flow from the counter electrodes to the central working electrode. This configuration has advantages concerning the ability of defining and focusing the superficial excitation sites of a nerve [46]. In order to restrict the excitation to deeper nerve areas and block non-requested superficial fibers, transverse steering currents can be applied by a multipolar electrode configuration, as shown in Fig. 2.9(d) [46].

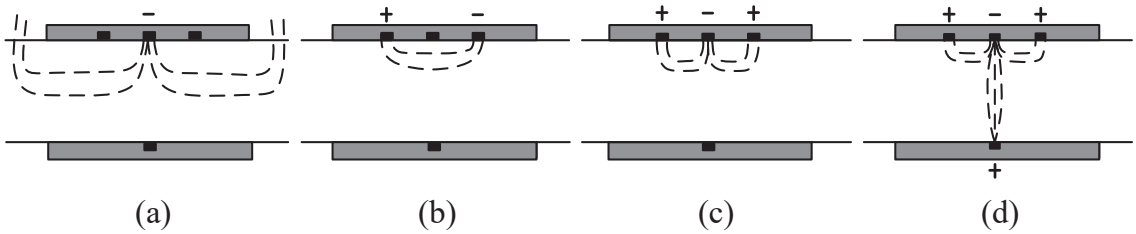


Figure 2.9.: Electrode configuration for, (a) monopolar, (b) bipolar, (c) tripolar, and (d) multipolar stimulation using steering currents. Reproduced and modified from [46] (©1990, IEEE).

2.3. Electrode-Tissue Interface

Electrodes represent the interface between stimulator circuit and excitable tissue. During stimulation a current transfer at the phase boundary from electron conduction in the solid state (metal) to ion conduction in the fluid state (electrolyte) takes place. According to the charge transfer mechanisms at the phase boundary, the equivalent electrical model of the electrode-tissue interface is derived.

2.3.1. Charge Transfer at the Phase Boundary

The two main charge transfer mechanisms at the phase boundary of the electrode-tissue interface are: capacitive charge redistribution, and Faradic reactions, illustrated in Fig. 2.10(a). In contrast to Faradic reactions, the charge transfer via capacitive mechanism happens without any crossing or exchange of charge carriers at the phase boundary. Carriers of opposing polarity, electrons in metal and hydrated protons in electrolyte, accumulate at the phase boundary, separated by a dielectric layer of water. The capacitive arrangement of these layers is known as the Helmholtz double layer. Charging and discharging of the Helmholtz double layer is completely reversible, the charge transfer takes place without any electrochemical reactions nor electrode or tissue damage. Therefore, the capacitive charge redistribution is the preferred charge transfer mechanism for successful and safe stimulation. The capacitive mechanism dominates at a small voltage across the phase boundary for a small amount of charge. The charge density capacity of a smooth surface metal electrode is up to $20\,\mu C/cm^2$. If the injected or withdrawn charge exceeds this density limit, the excess charge is transferred by Faraday currents [43]. Thereby, charge carriers cross the phase boundary, leading to reduction and oxidation (redox) reactions. Reduction, the addition of electrons, occurs at a negatively charged electrode (cathode), while oxidation, the removal of electrons, takes place at a positively charged electrode (anode).

One can distinguish between reversible and irreversible Faradic reactions. Reversible reactions are stationary, thus, the reactants stay near the electrode surface. Reversible mechanisms include oxide formation or reduction and hydrogen plating at platinum or other noble metals like iridium [43]

$$Pt + H_2O \longleftrightarrow PtO + 2 \cdot H^+ + 2 \cdot e^- \,, \tag{2.2}$$

$$Ir + 2 \cdot H_2O \longleftrightarrow Ir(OH)_2 + 2 \cdot H^+ + 2 \cdot e^- \,. \tag{2.3}$$

The surface redox reactions might change the oxidation state of the metal oxide, however, they do not create new chemical species in the biological tissue and are reversed by changing the polarity of the applied stimulus. The overall chemical composition remains unchanged, and therefore, the reversible Faradic reactions are considered as physically harmless [2, 43].

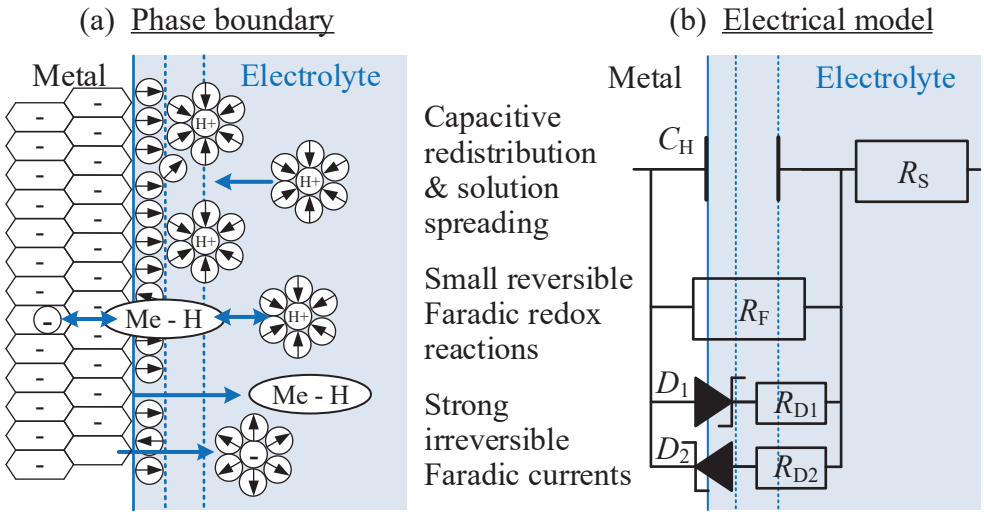


Figure 2.10.: The phase boundary of the electrode-tissue interface describing (a) the charge transfer mechanisms and reactions (reproduced and modified from [43]), and (b) the equivalent electrical model.

Irreversible Faradic redox reactions arise in case of larger permanent currents or voltages across the electrode-tissue interface. In this case, the mass transport rate dominates the electron transport rate in the electrolyte, and the resultant reaction products diffuse into the solution (Fig. 2.10). Irreversible mechanisms include also electrode corrosion

$$Pt + 4 \cdot Cl^- \longrightarrow [PtCl_4]^{2-} + 2 \cdot e^- \tag{2.4}$$

and electrolysis of water, leading to hydrogen or oxygen evolution

$$2 \cdot H_2O + 2 \cdot e^- \longrightarrow H_2 \uparrow + 2 \cdot OH^- , \tag{2.5}$$

$$2 \cdot H_2O \longrightarrow O_2 \uparrow + 4 \cdot H^+ + 4 \cdot e^- , \tag{2.6}$$

where the symbol (↑) indicates gas evolution. These reactions alter the composition of the electrode surface and generate toxic reaction products with pH change of the surrounding solution. In summary, irreversible Faradic reaction are unwanted charge injection processes and must be circumvented during electrical stimulation, since they cause damage to both, the electrode and the tissue [2, 43].

2.3.2. Equivalent Electrical Model

Based on the charge transfer mechanisms at the phase boundary, an equivalent electrical model of different types of electrical components can be derived, as shown in Fig. 2.10(b). The charge accumulation at the phase boundary that forms the

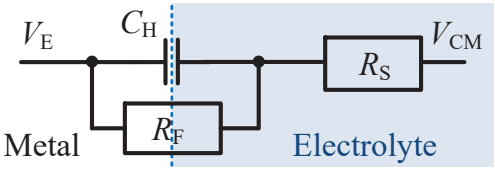


Figure 2.11.: Simplified equivalent electrical model of the phase boundary.

Helmholtz double layer and builds up a potential difference, exhibits the behavior of a parallel plate capacitor. The parallel plate capacitance

$$C_H = \varepsilon_0 \cdot \varepsilon_\mathrm{r} \cdot \frac{a}{d_\mathrm{H}}\,, \tag{2.7}$$

with electric constant ε_0, relative permittivity of electrolyte ε_r, and d_H the thickness of the Helmholtz double layer, depends mainly on the electrode surface area a [43]. Additionally, the electron conduction in metal is transferred into ion conduction in electrolyte, the latter is modeled by the solution spreading resistance R_S in series to C_H. Further, a resistance R_F is introduced in parallel to C_H, representing reversible Faradic currents. The technical implementation for strong Faradic currents is the parallel connection of two Zener diodes D_1 and D_2, modeling irreversible positive and negative currents, respectively. More complex model descriptions, e.g. considering diffusion of the chemical reactants in solution by the Warburg impedance, can be found in [43]. However, for safe stimulation, which implies that the voltage across the tissue interface is kept low and strong Faradic currents are prevented, the electrode-tissue interface is simplified to the model shown in Fig. 2.11. Its complex impedance Z, with respect to the stimulation frequency ω

$$Z(\omega) = \left(\frac{1}{R_\mathrm{F}} + jwC_\mathrm{H}\right)^{-1} + R_\mathrm{S}\,, \tag{2.8}$$

describes the current-voltage behavior at the electrode as a first order high pass. The electrode values vary depending on the material and geometry [9]. The equivalent model parameters of a cuff electrode and given values from literature are listed in Tab. 2.1. The equivalent model parameters of the cuff electrode are extracted from data of an impedance measurement over a frequency sweep, using the fitting tool of the software program MATLAB for Eq. (2.8). However, uncertainties about the extracted impedance values are still an issue due to tissue growth and electrode migration after surgery [47].

2.3.3. Remaining Charges and Safety Limits

The charge density, which is the total charge divided by the area of C_H, must be kept below a critical charge limit to ensure save charge injection during stimulation. The reversible charge injection limit, also referred to as water window, depends mainly

Table 2.1.: Parameters of the equivalent electrical model for different types of electrodes.

type	cuff* [7, 8]			retinal [4]			retinal [48]	wire [49]
material	Pt coated with IrO2			Pt black			IrO2	Pt-Ir
size in mm^2	0.075 working	0.425 reference	1.225 anode	0.002	0.031	0.785	-	'tip area'
C_H in µF	0.5	7	20	0.022	0.11	5.5	1.1	0.2
R_S in kΩ	3	1.5	1.0	8.72	3.46	1.15	1.1	10
R_F in kΩ	150	20	15	-	-	-	>10 000	500

* extracted from measurements

on the material of the electrode and can be defined during cyclic voltammetry [43]. The water window of platinum electrodes, for example, lies between −600 mV and 800 mV [50]. Therefore, safe electrical stimulation considers stimulation parameters that keep the charge density of each stimulus within the water window for the chosen electrode type. However, application-specific stimulation parameters are only one part of the solution for safe stimulation. Additionally, ideal safe electrical stimulation requires zero residual charges across the electrode-tissue interface to avoid the transfer of net charge that might lead to irreversible Faradic reactions.

Residual charges are related to the remaining electrode voltage V_E across the electrode-tissue interface with respect to the body's quiescent potential V_{CM}. The development of residual charges is shown at an example of a monophasic rectangular stimulus with intensity I_0 and pulse width t_w, and its corresponding voltage waveform in Fig. 2.12. The generated voltage at any time $t < t_w$ is mathematically described by

$$V_E(t) = I_0 \cdot R_s + I_0 \cdot R_F \cdot (1 - e^{\frac{-t}{R_F C_H}}), \quad t_0 \leq t < t_w, \tag{2.9}$$

where the initial voltage increment equals the voltage drop across R_S due to the steep transient increase of I_0. The second term results from I_0 gradually charging C_H. Ideally, for R_F towards infinity, this part exhibits ideal integration

$$V_{E,int} = I_0/C_H \cdot t_w, \tag{2.10}$$

with linear voltage increase during t_w. However, for a finite value of R_F, Faradic current through R_F conducts a portion of the injected current I_0, causing a nonlinear voltage increment, which approaches $I_0 R_F$, with time constant $R_F C_H$. The abrupt stop of I_0 through R_S at the end of the stimulus results in a sudden voltage drop. The resultant V_E then corresponds to the charge stored in C_H and diminishes only

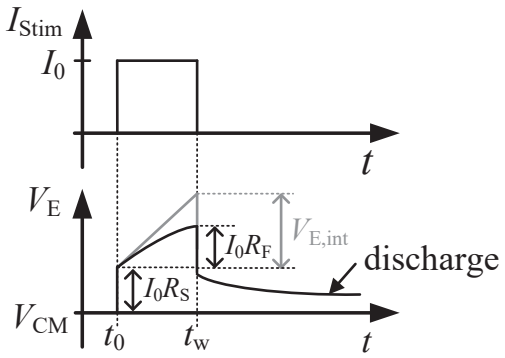


Figure 2.12.: The corresponding voltage waveform for a monophasic rectangular current pulse across the equivalent electrical model.

slowly with time

$$V_E(t) = \left(I_0 \cdot R_F \cdot (1 - e^{\frac{-t_w}{R_F C_H}})\right) \cdot e^{\frac{-t}{R_F C_H}}\,, \quad t \geq t_w\,, \tag{2.11}$$

by passive discharge through the resistive path. [50, 51]

A common approach to avoid large remaining voltages is to use biphasic stimulation pulses instead of a monophasic pulse. An ideal biphasic stimulation provides equal amount of cathodic and anodic charges. After each stimulus, V_E safely returns and stays at the reference potential V_{CM}, as shown in Fig. 2.13(a). However, in reality, mismatch between the cathodic and anodic charge packages, illustrated by ΔQ in Fig. 2.13(c), inevitably occurs due to process variations. Moreover, [50] emphasizes that even with matched biphasic current pulses a residual voltage V_E exists, due to leakage current via R_F if the delay time t_d is not zero (Fig. 2.13(c)). Including the effect of a non zero t_d and assuming a mismatch in the biphasic waveform leads to a residual voltage V_E of

$$V_E = \left(-I_c \cdot R_F \cdot (1 - e^{\frac{-t_{wc}}{R_F C_H}}) \cdot e^{\frac{-t_d}{R_F C_H}} + I_a \cdot R_F \cdot (1 - e^{\frac{-t_{wa}}{R_F C_H}})\right) \cdot e^{\frac{-t_{dis}}{R_F C_H}}\,, \tag{2.12}$$

at the end of one stimulation cycle. Usually, t_d is short and R_F large, which diminishes its effect on the residual voltage V_E compared to a mismatch in stimulation amplitude I_a and I_c or pulse width t_{wa} and t_{wc}. During t_{dis}, C_H discharges passively through R_F. However, a complete discharge is only possible, if t_{dis} is sufficiently long

$$t_{dis} \gg \tau_{dis} = R_F \cdot C_H\,. \tag{2.13}$$

Otherwise, an offset potential at the beginning of a subsequent stimulus exists. Charge accumulation of further stimulation cycles intensifies the problem. Without compensating the excess charges, a dangerous voltage level will be reached, leading to irreversible Faradic reactions. Therefore, predefined safety limits of $\pm 50\,\text{mV}$ [6] or $\pm 100\,\text{mV}$ [4, 9], well below the water window, are considered around the neurons' quiescent potential V_{CM}, within which V_E is tolerable.

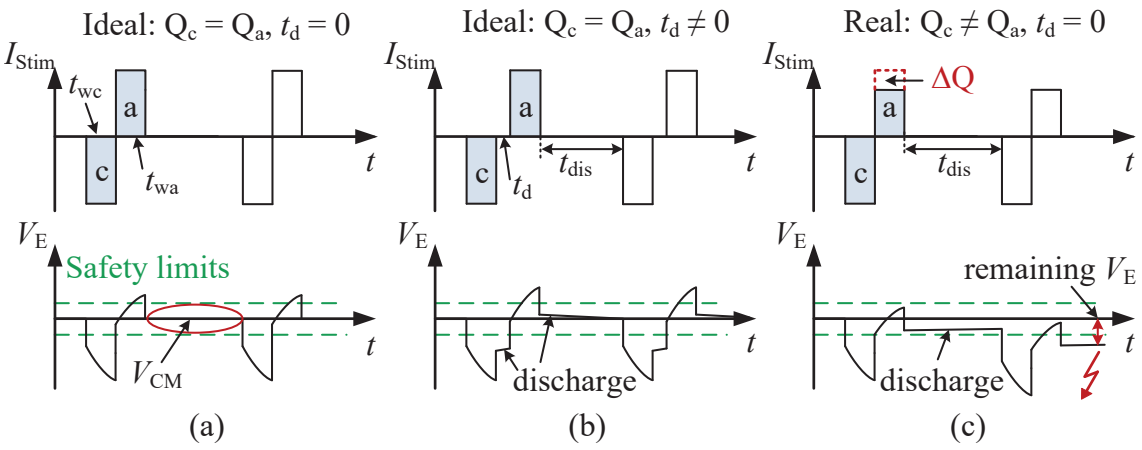


Figure 2.13.: Comparison between (a) ideal biphasic stimulation, (b) biphasic stimulation including delay time t_d, and (c) real biphasic stimulation with current mismatch ΔQ leading to dangerous remaining electrode voltages.

2.4. Summary

Although APs are generated physiologically, the excitation of nerves can be artificially triggered by injecting electrical charges into excitable tissue, and thus, changing the transmembrane resting potential. Different charge delivery strategies are discussed in this chapter. Among these, the current-controlled stimulation is favored, since it allows for a good control of the transferred charge, regardless of impedance variations. Electrodes represent the interface between stimulator circuit and biological tissue. Different types of electrodes are exemplarily introduced. Further, it is explained how an appropriate configuration of the active electrodes of an electrode array, increases the spatial selectivity for the excitation of the selected fiber within a nerve.

A first approach for tissue and electrode protection is using biphasic stimulation pulses that ideally reverse all electrochemical reactions at the phase boundary. However, any monophasic or unbalanced biphasic stimulus causes residual net charges across the electrode-tissue interface, leading to irreversible Faradaic reactions with toxic byproducts causing pH changes and electrode dissolution. Therefore, any residual charge must be monitored and controlled. A measure for the residual charge is the remaining electrode voltage V_E. With respect to the application and electrode material safety limits are defined, in which V_E is tolerable. At this point charge balancing becomes indispensable, as it keeps V_E within these predefined safety limits. An equivalent electrical model of the electrode-tissue interface is derived by having a closer look at the charge transfer mechanisms of the phase boundary. The model is simplified to three main components, which are the Helmholtz double-layer capacitor C_H, a solution spreading resistance R_S, and the Faradaic resistance R_F.

3. State-of-the-Art Charge Balancing

Safety in neural electrical stimulation is a major theme addressed by nowadays scientists. There exist different approaches for electrode and tissue protection, which ensure that no net charge is transferred at the electrode-electrolyte interface. This chapter summarizes state-of-the-art charge balancing methods. An overview about the different charge balancing categories is given in Fig. 3.1. Beside the attempt to decouple DC voltages at the electrode by blocking capacitors, closed loop charge balancing systems compensate residual charges by comparing the remaining electrode voltage V_{E} to the body's quiescent potential V_{CM}. In the group of closed loop charge balancing, we distinguish between two compensation methods that differ in their mode of action. The consequence-based approach aims for an instantaneous reduction of V_{E} above the safety limit, after each stimulus. The cause-based methods counteract mismatch and process variations and ensure a long-term balanced condition, for example, by adjusting the charges of the anodic and cathodic stimulus, typically averaged over many pulses. After a general introduction of previous methods, the thesis concentrates on the methods marked in red. A detailed description about their principles, designs and measurement results are given in the subsequent chapters.

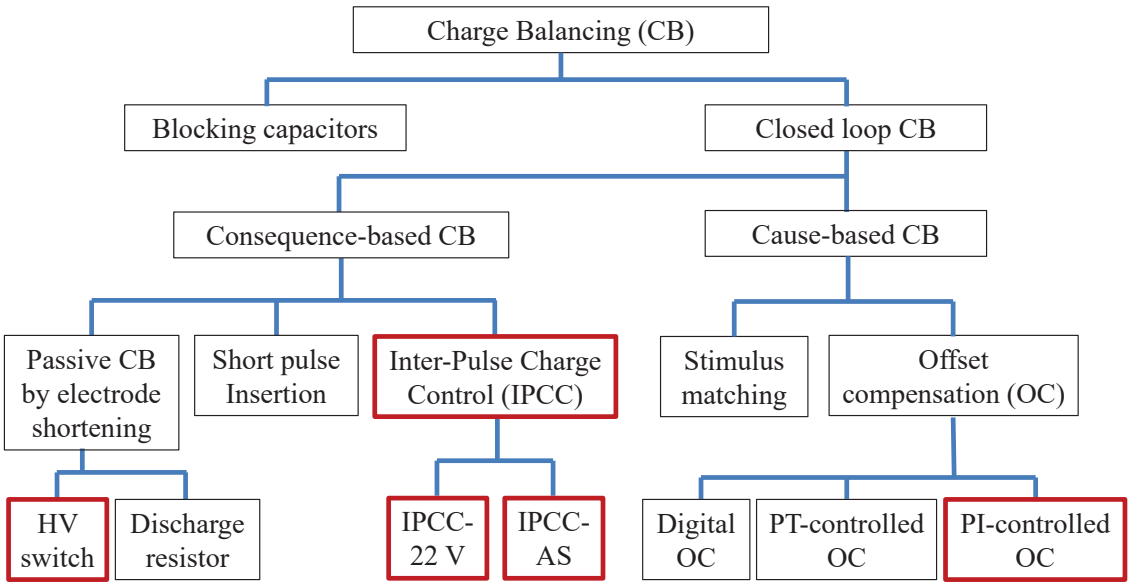


Figure 3.1.: Overview of state-of-the-art charge balancing categories.

3.1. Blocking Capacitors

Introducing a blocking capacitor C_{block} in series to the electrode, as illustrated in Fig. 3.2, is often argued [40, 52, 53] to protect the tissue against net currents. Maximum allowed net currents are defined in [54], being determined by observing tissue damage and relating it to an overall net current, calculated by current integration over time. However, the influence of the electrode impedance, e.g. the amount of charge accumulation and the capability of self-discharge, is neglected. Therefore, the derived current limits are not universally valid, on the contrary, they vary considerably from one application to another.

Having a closer look at the effectiveness of a blocking capacitor by considering voltage and current mode stimulation makes clear that it is not a sufficient protection method. In the case of voltage mode stimulation, C_{block} isolates V_{E} from the DC level of V_{Stim} on the circuitry side. Thus, a self-discharge at the electrode via R_{F} can take place until V_{E} equals V_{CM}. Nevertheless, fast switching events and AC voltages (like stimulation pulses) will pass C_{block} and may lead to an unwanted residual voltage V_{CH} across the Helmholtz capacitor C_{H}. Considering current mode stimulation, any AC currents and erroneous DC offset currents are being integrated not only at C_{block} but also at C_{H}, thereby mobilizing ions in the tissue that accumulate at the phase boundary, as illustrated in Fig. 3.2. Therefore, introducing a blocking capacitance will not protect the electrode from the development of a residual voltage V_{CH}, as it is demonstrated in Fig. 3.3(a). Only in case of a permanent net current, shown in Fig. 3.3(b), that causes V_{Stim} to reach a constant voltage level, e.g. the supply V_{DD}, blocking capacitors are reasonable since they interrupt the integration process at C_{H} and allow for a complete self-discharge of V_{CH}.

Furthermore, an additional voltage drop across C_{block}, V_{Cb} illustared in Fig. 3.2, is induced during stimulation, and increases the voltage overhead of V_{Stim} required for successful stimulation. Therefore, C_{block} must be chosen significantly larger than C_{H} to result in a voltage drop that is negligible small compared to the one across C_{H}

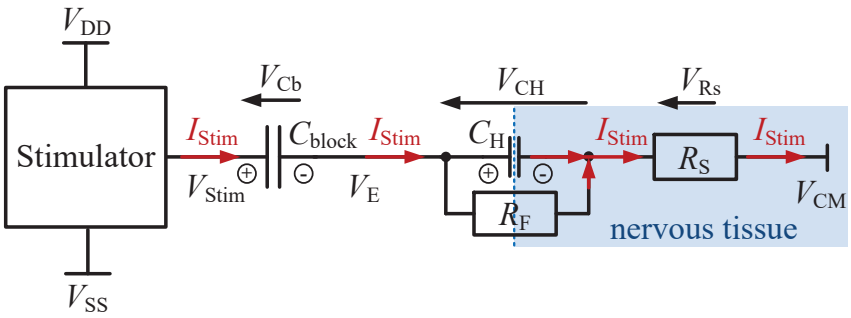


Figure 3.2.: Schematic of the system setup with a blocking capacitor C_{block} at the output of the stimulator, illustrating the additional voltage drop V_{Cb} that is induced within the signal path.

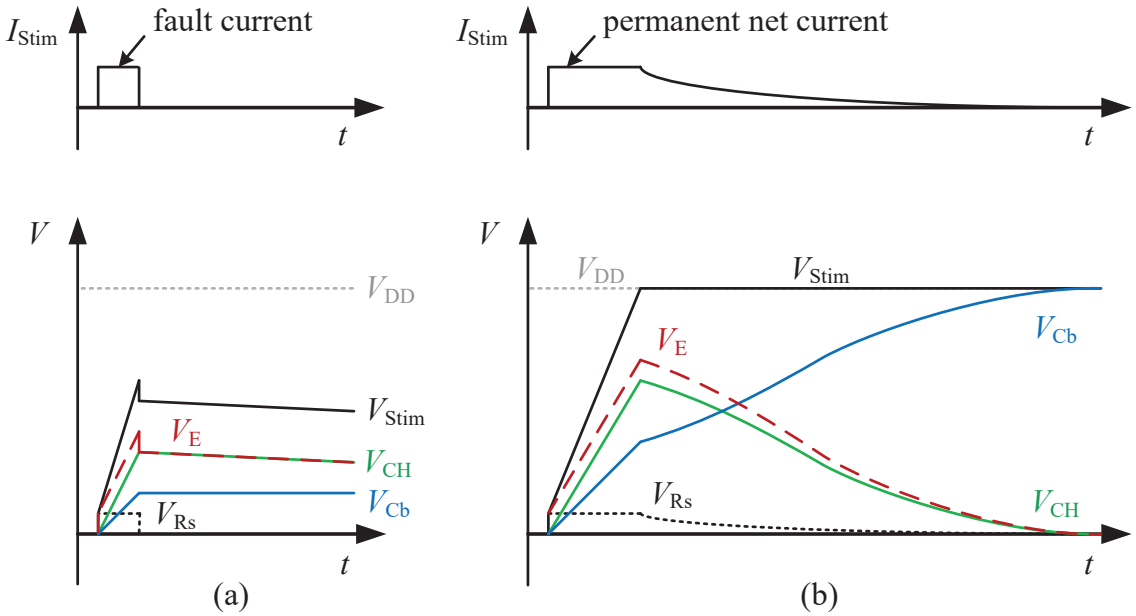


Figure 3.3.: Schematic signal diagram, describing in (a) the irrelevance of C_{block} in case of fault AC or DC currents, and in (b) the positive effect of C_{block} on the electrode voltage V_E for net currents once V_{Stim} stays constant, i.e. due to clipping.

[40]. Blocking capacitances are expected in the range of 1 µF to 100 µF and have to be realized off-chip bringing along disadvantages in terms of area and assembly. Additionally, a regular discharge of C_{block} is necessary to avoid voltage saturation.

Even though, using blocking capacitors is an accepted method, and practiced in many certified medical devices, it can be stated that C_{block} has disadvantages in terms of area and effectiveness. It is neither a sufficient protection nor an alternative to CB in current mode stimulators.

3.2. Consequence-Based Charge Balancing Methods

The consequence-based compensation methods aim for an instantaneous discharge of the remaining electrode potential by inserting additional charges of opposite polarity to the electrode or allow for an electrode self-discharge. The imbalance in the stimulus itself stays untouched. Therefore, once accumulated charges at the electrode become critical, compensation after each stimulus is required continuously.

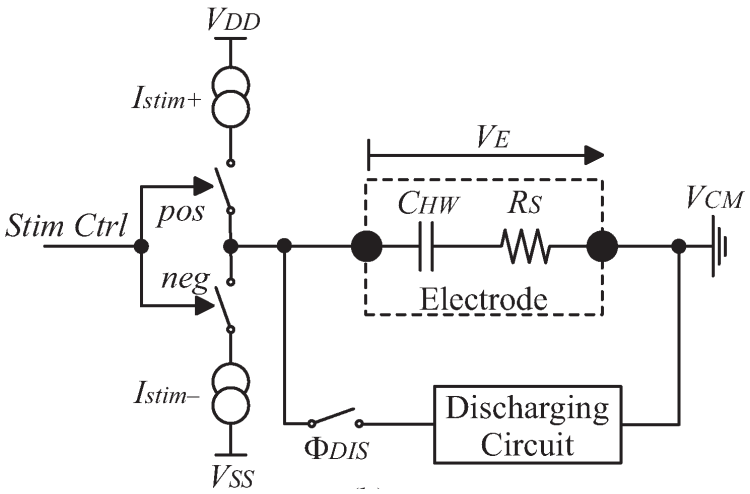


Figure 3.4.: Passive charge balancing by shorting the electrode via a discharge resistor or a similar discharging circuit. Taken from [9] (©2010, IEEE).

3.2.1. Passive Charge Balancing

One subgroup of the consequence-based compensation methods is passive CB, such as electrode shorting by discharge resistors [27, 55], shown in Fig. 3.4. However, its success and compensation current intensities are not controlled [40]. They depend on the amount of residual charge, the time available for discharge and its time constant, defined by the electrode impedance and discharge resistance [40, 56]. Especially, considering multi-channel FES, passive CB brings disadvantages not only in terms of size but also in efficacy [40, 56]. For example, the effectiveness of stimulation is reduced in case that one channel is stimulated, while an adjacent channel is shorted to V_{CM}, thus creating and unwanted current path through a second electrode [56]. Additionally, several electrodes shorted simultaneously to V_{CM}, distribute their charges among each other in an uncontrolled manner, in which current peaks might trigger action potentials. Further, HV stimulation also requires HV-robust CB circuits. Thus, even simple solutions like electrode shorting bring along challenges, i.e. the lack of HV switches [5, 40]. Therefore, in chapter 4, this work gives a solution for passive CB via a HV-robust switch.

3.2.2. Short Pulse Insertion

One subgroup of consequence-based CB is short pulse insertion of a fixed amount of charge [4, 6, 9, 48]. In between the stimulation periods, the residual electrode voltage V_{E} is monitored and compared to the predefined safety limits. Once the safety limit is exceeded, short current pulses are inserted into the electrode, as shown in Fig. 3.5. In [6] for example, the pulses have an amplitude of $\pm 20\,\mu\mathrm{A}$ and a width of $20\,\mu\mathrm{s}$. The duration of the required balancing period is estimated by an off-chip microcontroller.

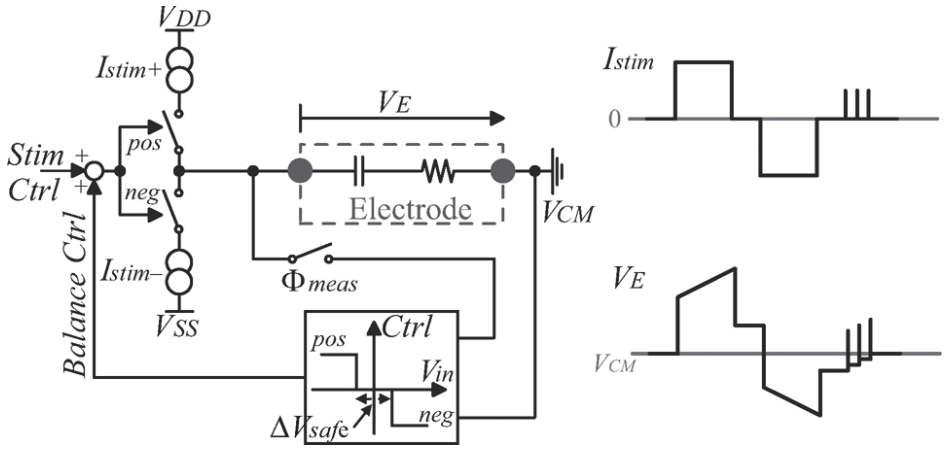


Figure 3.5.: Short pulse insertion charge balancing and its waveforms. Taken from [9] (©2010, IEEE).

In addition to control units, further components like comparators are necessary to determine the safety limits and the direction of compensation.

Short pulse insertion is further examined in [9]: "Nonetheless, the effect of the inserted short pulses on an unwanted neural stimulation has not been proven yet. In addition, the required number of balancing current pulses and, therewith, the duration of the charge balancing depends on the actual charge imbalance after each stimulation. Vice versa, the maximum amount of mismatch charge, which can be compensated, depends on the adjusted charge per pulse and the number of pulses allowed over time." The pulse insertion control loop is stable and the electrode potential is settled within the safe range only, if the time between two stimulations is long enough to fit the required number of balancing pulses and if the charge of these pulses is small enough not to exceed the safety range.

3.3. Cause-Based Charge Balancing Methods

Cause-based compensation methods aim to mitigate the origin of the charge mismatch within the stimulator. Instead of an instantaneous charge compensation, a long-term balanced condition is reached by charge correction of the cathodic and anodic stimulus. Thereby, the amplitude or pulse width of the stimuli are adjusted by a preceding settling process with possible overshoots during startup. The two subgroups stimulus matching and offset compensation differ in their reference for successful compensation, which is the surveillance of the transferred charges or the residue electrode voltage, respectively.

3.3.1. Stimulus Matching

Stimulus matching, as proposed in [27, 31, 42, 57], adjusts the biphasic stimulation pulse based on the surveillance of the transferred charges. However, these charge balancing techniques rely on active measurements of the biphasic current pulses or well matched circuits, and thus, are not a feasible alternative [9]. In [58] and [59] the idea is to avoid mismatch between anodic and cathodic charges by switching a single floating current source, shown in Fig. 3.6. However, derived maximal charge errors [59] or residual precision of the matched current sources [27, 31] are not crucial criteria for save operation. On the contrary, these specifications vary considerably from one application to another, since the effect of the residual charges on the actual electrode has to be considered. Further, even with perfectly matched cathodic and anodic charges, a zero residual charge at the electrode will not be achieved, due to disturbances on the electrode voltage, e.g. by crosstalk of adjacent electrodes, and self-discharge during inter-pulse delays [56]. Additionally, electrochemical processes at the phase boundary differ for positive and negative charges, which causes an additional kind of asymmetric charge leakage. Therefore, as experimentally showed in [60] and also stated in [9] "... limiting the electrode potential to within safe limits is a more important objective than achieving a well-balanced stimulation waveform."

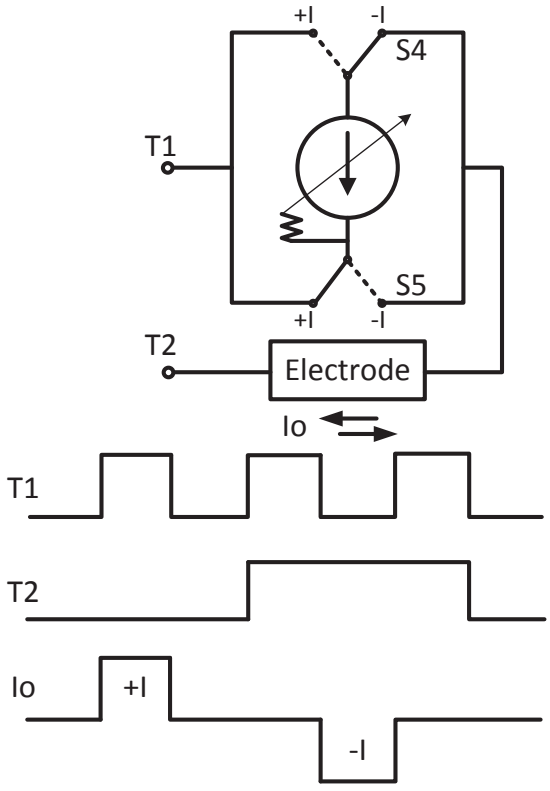


Figure 3.6.: Stimulus matching by using a single floating current source. Taken from [58] (©2011, IEEE).

3.3.2. Offset Compensation

Offset compensation (OC) methods balance remaining charges by supplying an offset current in the background, depending on the monitored residual electrode voltage V_E [4, 9, 56]. Thus, in contrast to the pulse matching technique, the above mentioned disturbances and unwanted processes at the electrode-tissue interface are recognized and incorporated.

Analog Offset Compensation: For analog OC, the offset current can either be supplied continuously by an additional current source, or by adjusting the cathodic or anodic current amplitude [9] or pulse width [56]. V_E is monitored after each stimulation and might be compared to the safety range, as shown in Fig. 3.7. However, in difference to the pulse insertion, remaining charges are not compensated directly after each stimulus. It takes an initial settling process to adjust the offset current

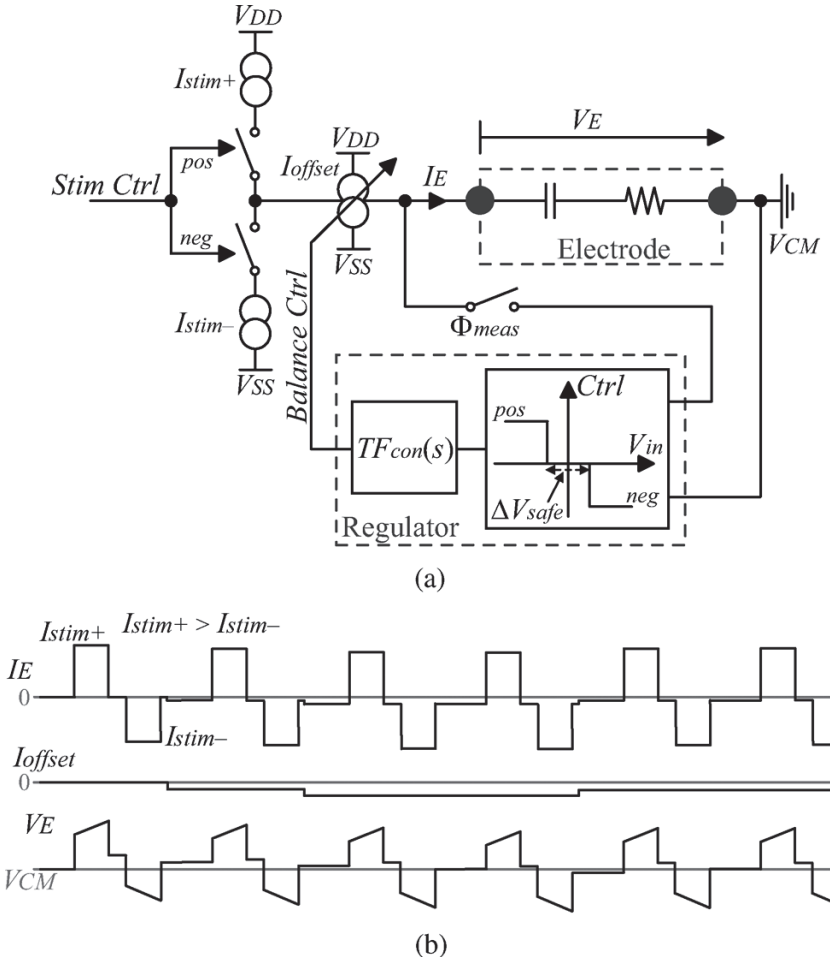


Figure 3.7.: (a) Analog offset compensation, and (b) its waveforms based on permanent background balancing. Taken from [9] (©2010, IEEE).

to match the biphasic stimulation pulse, which works well in continuous systems for chronic implantation. However, this approach is not suitable for compensating fast transient events, which might arise during seldom stimulation (e.g. implantable cardioverter-defibrillator). Analog offset compensation balancers must provide an integration time constant which is larger than the stimulation period to ensure a "memory" like behavior of the offset value for multiple stimulation pulses. The time constant must be in the order of a few milliseconds, requiring large RC-values. Therefore, the proposed offset compensation of [9] was realized on a printed circuit board (PCB) using discrete components. For an ASIC implementation, however, different approaches must be found to realize the RC-values of the proposed integrator, otherwise these would lead to an unrealistic large chip area. Additionally, the controller proposed in [9] is a non-ideal I controller (PT controller), representing a one pole system. In combination with the electrode's transfer behavior, this controller choice might not be convenient considering stability and special care must be taken during controller dimensioning, as discussed in sec. 5.4.

Digital Offset Compensation: The digital OC, as implemented in [4], avoids large RC-values by replacing the analog integrator of [9] with a 3-bit Moore state machine, to control two additional offset current sources. Therefore, the residual V_{E} is compared to a reference voltage by a HV window comparator after each stimulus. Within the safety range, the state machine remains at its current state. Once a safety limit is exceeded, the state machine moves one state up or down and the offset current is increased or decreased by one least-significant-bit (LSB) dependend on the mismatch direction, illustrated in Fig. 3.8. The implementation of [4] allows

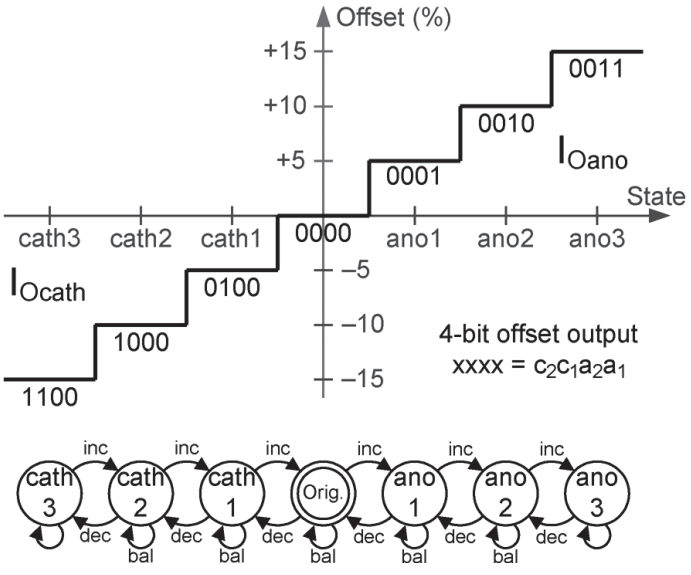


Figure 3.8.: Digital offset compensation by a 3-bit state machine to control additional offset current sources I_{Ocath} and I_{Oano}. Taken from [4] (©2012, IEEE).

to correct for ±15% biphasic current mismatch. However, the digital offset compensation is limited by the total amount of compensation charges and by its precision according to the number of bits.

3.4. Summary

Charge balancing has become an integral part of neural interfaces since it protects against electrode corrosion and tissue damage. This chapter categorizes and discusses different types of state-of-the-art charge balancing methods. Nowadays most certified medical devices are equipped with blocking capacitors and passive charge balancing, despite their disadvantages of size and uncontrolled balancing, concerning charge compensation time and efficacy. A promising alternative for small, fast, and controlled charge compensation is the active charge balancing, based on the surveillance of the remaining electrode voltage after stimulation. Consequence-based methods like short pulse insertion are advantageous for instantaneous charge balancing. However, the possibility of an unwanted stimulation has not been proven yet. Further, the charge packages per pulse must be small enough to not exceed the safety range, otherwise instability with toggling might be the case. Cause-based offset compensation is a promising method to achieve a stable long-term balanced state. Great care must be taken with the controller design considering settling behavior and stability. Digital compensation has a limited precision according to the applied number of bits. Analog approaches on ASIC level implementation are challenging in the realization of the controller and are not yet reported by others.

4. Overall System Description and Stimulator Front-End

Implantable stimulation devices, as illustrated exemplarily in Fig. 4.1, are typically provided with data and energy by a large radio frequency (RF) induction coil. They contain a power management, a monitoring circuitry (Sense), a microcontroller unit (µC), and a stimulator front-end including charge balancing (Stim+CB) that is attached to appropriate electrodes. This chapter[2] comprises Stim+CB only and starts by showing the conceptual configuration of the stimulator front-end with the proposed charge balancing circuits that interface at the electrode. Due to the HV stimulation environment, all circuits and components must be HV compliant. Therefore, a quad-rail methodology is introduced that allows for HV compatible, power-efficient, and supply rail independent designs.

All system simulations and measurements presented in this thesis are based on the proposed stimulation setup using the stimulator front-end and the HV switches that

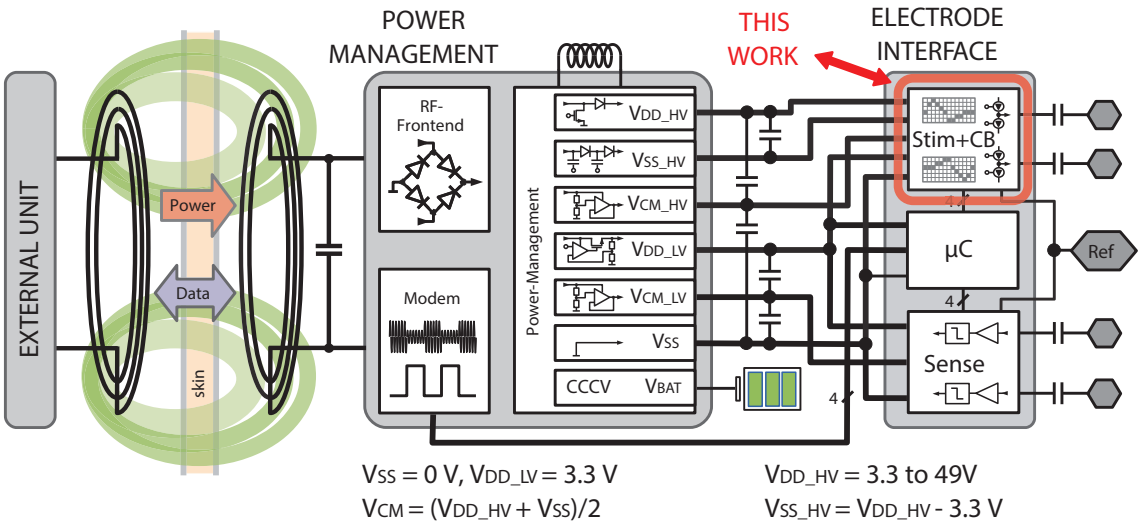


Figure 4.1.: The current-controlled stimulator front-end (highlighted) used in an implantable electronic device. Labels adjusted from [61] (©2018, IEEE).

[2]The contribution of the author to the shown device (Fig. 4.1) involves the stimulator's analog front-end and charge balancing (Stim+CB) only [61]. The author supplied passive and active charge balancing, on the latter lies the main focus of this thesis. The content of this chapter is partially published in [62] and [13, 61, 63] (©IEEE).

are introduced in this chapter. Investigations and results of the implemented stimulator front-end are described regarding HV robustness, low-power consumption, and flexibility in terms of arbitrary waveform generation. The HV compliant switches are important interface components, since they separate the charge balancing circuits from the stimulator circuitry. Further, the same HV switch architecture, however designed with different dimensions, is used for passive charge balancing, shorting the electrode via its on-resistance.

4.1. System Setup

An overview about the conceptual configuration of the stimulation setup including charge balancing, as implemented in this work, is shown in Fig. 4.2. The current-controlled stimulator periodically releases biphasic pulses I_{Stim}, according to the digitally preprogrammed signal C_{trl}, onto the electrode-tissue interface. Cause-based and consequence-based CB techniques were implemented to compensate for accumulated residual charges that remain in the tissue interface. These CB methods can be activated independently, or in a cause-based and consequence-based CB combination via S_1 and S_2, or S_P. The signal diagram in Fig. 4.2 illustrates the timing of the CB switches with respect to the stimulation switches S_a and S_c for a combined use of cause-based and consequence-based CB. The initial state of $S_{1,2,P}$ is 'open', ensuring that during stimulation all charge balancers stay inactive. Directly after the stimulus, S_1 is high for a short interval. Thus, the cause-based balancer monitors V_E and steers its current driver that interferes with the stimulator to adjust I_{Stim}. Subsequently, one of the consequence-based balancers is activated by either S_2 or S_P, which stays high until the next stimulus starts, thus being able to react to disturbances. In case of active consequence-based CB, V_E is monitored and an additional current driver instantaneously compensates remaining charges.

The variability of current amplitudes and respective electrode impedances during stimulation requires high adaptability in terms of supply voltage compliance. In case of small electrodes with high impedance, typically larger than 1 kΩ [4], HV compliance of the stimulator is needed. Voltages between 4.6 and 30 V are reported in [4, 6, 9, 31]. Due to this HV environment, all CB circuits as well as all interface switches require robust HV compliance. To accommodate the variability in electrode impedance and patient threshold it can be stated that a higher compliance voltage of the stimulator will offer a more general usability. Therefore, this work aims at achieving a reasonable high voltage compliance of 30 V to 40 V that is possible in the employed 0.35 µm HV CMOS technology.

Considering an implantable device as shown in Fig. 4.1, the induced voltage, from the transmitter coil to the receiver coil, is expected to be small. Therefore, the induced voltage must be boosted to drive the HV stimulator circuitry. Thus, the energy efficiency is reduced, which makes energy saving techniques crucial. Publications are usually focusing on the efficiency of the stimulation pulse, trying to minimize

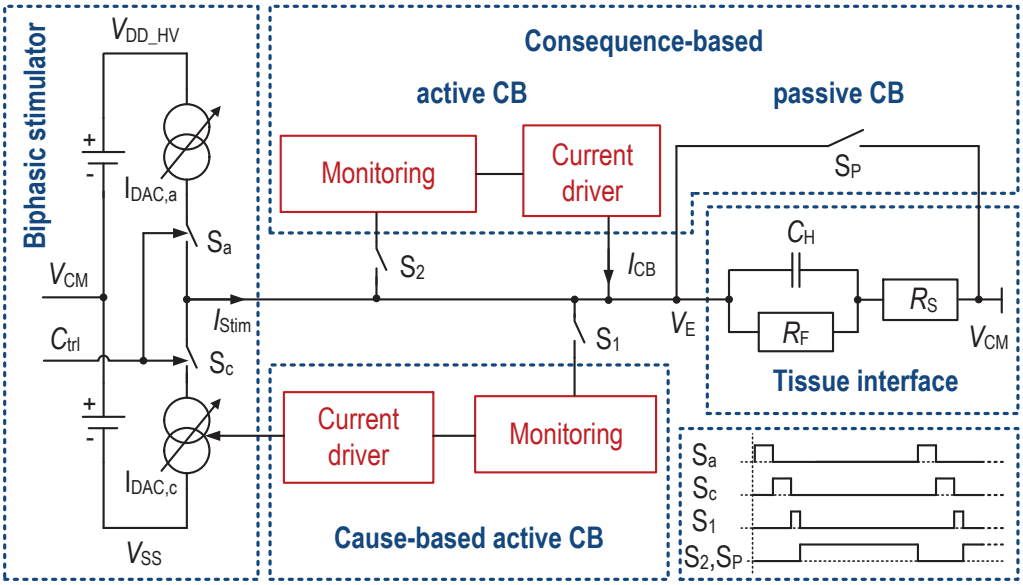


Figure 4.2.: System overview of the biphasic current-controlled neural stimulator front-end, consequence-based and cause-based charge balancing and the electrical equivalent model of the electrode-tissue interface.

the power-losses during the pulse period [6]. This is reasonable if the stimulation frequency is sufficiently high. However, in the applications considered in this thesis, the stimulation takes place in periods of around 10 ms to several seconds only. In each case the stimulator has to react immediately, and a time-consuming wake up phase has to be avoided. Thus, the overall energy consumption is dominated by the circuit's static power consumption. Therefore, the systems architecture was optimized for low static power consumption. Additionally, a quad-rail methodology that allows adjusting the supply to the minimum needed is applied in the stimulator design (sec. 4.3) and in the latest design of a consequence-based active CB (chapter 6).

4.2. Quad-Rail Methodology

The principle of quad-rail methodology is depicted in Fig. 4.3. The voltage levels are exemplary given for the stimulator described in sec. 4.3. The quad-rails represent four supply rails V_{SS}, V_{DD_LV}, V_{SS_HV}, and V_{DD_HV}. The supplies V_{SS} and V_{DD_LV}, as well as V_{SS_HV} and V_{DD_HV}, define LV domains each, denoted as $\triangle V_{LV}$. Both $\triangle V_{LV}$ domains are fixed to 3.3 V. The lower domain is defined with respect to the lowest potential V_{SS} and the upper domain with respect to the highest supply rail V_{DD_HV}. All LV transistors of the upper $\triangle V_{LV}$ domain may lie within the HV environment $\sum V_{HV}$ ($\hat{=}$ V_{DD_HV}). These transistors are then exposed to high bulk-substrate voltages, and therefore, are of isolated substrate type.

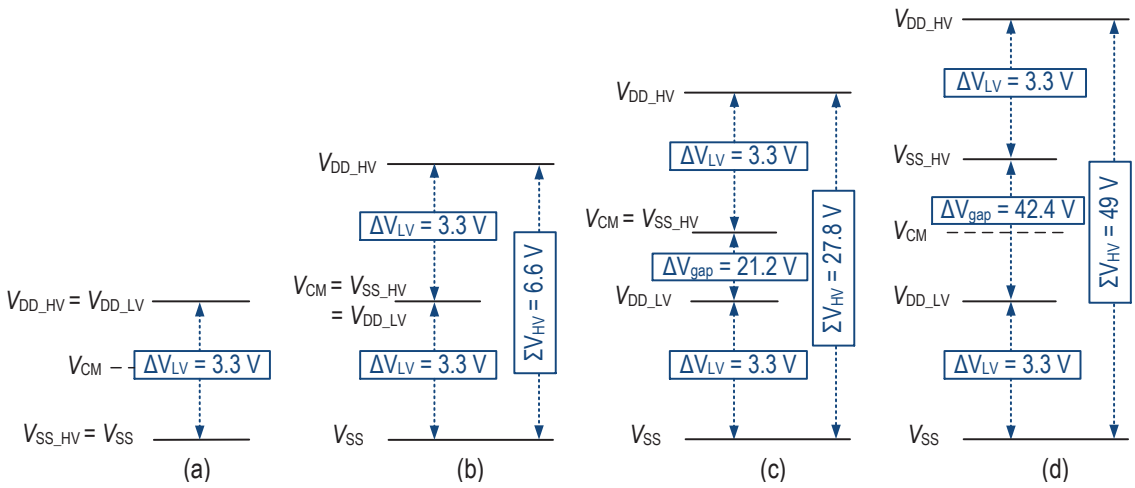


Figure 4.3.: Adaptive quad-rail methodology at (a) minimum possible supply range, (b) adjacent supply ranges, (c) asymmetric supply range displacement, and (d) maximum possible supply range.

The idea of the quad-rail methodology is to define LV sub-domains within the HV environment. The LV sub-domains contain most active circuit components, and protect these from HV. Additionally, die area can be saved since mainly LV transistors are used, whose minimum dimensions are 12 times smaller than those of the available HV transistors. Further, the operating characteristics become mainly independent of the outer HV supplies and power losses are reduced by adjusting the outer supplies for each application to the minimum voltage needed.

As illustrated in Fig. 4.3, the quad-rail methodology allows to shift the outer rails against each other without affecting the characteristics and efficacy of the low-voltage circuits, since these are depended on the $\triangle V_{LV}$ domains only. For the example of the stimulator (sec. 4.3), the circuit works for a voltage range $\sum V_{HV}$ that is variable from 3.3 to even 49 V. The body's quiescent potential V_{CM} serves as reference and lies usually between V_{SS} and V_{DD_HV}. As an additional feature, this methodology even supports an asymmetric supply range displacement with respect to V_{CM}. Some applications require different amplitudes for the cathodic and anodic pulse during biphasic stimulation. Using the supply range displacement, the stimulation efficiency can be improved by adapting the power supply according the needs of the application. For a monopolar stimulation for example, V_{CM} does not need to be symmetrical against the power rails. The cathodic supply range from V_{SS} to V_{CM} might be needed at the maximum to provide high stimulus currents, whereas V_{DD_HV} might be sufficiently high at 3.3 V above V_{CM} (Fig. 4.3(c)) or even equal to V_{CM}. Including this feature, the power consumption of the proposed stimulator is not only competitive to other bipolar stimulators [4, 6, 57], but also to monopolar simulators using an H-bridge configuration like [64].

4.3. Stimulator Front-End

The neural stimulator[3], shown in Fig. 4.4, contains six channels. The main building blocks of channel 05, for example, are framed in the chip layout of Fig. 4.5. They consist of the digital control, the digital level shifter, the static random-access memory (SRAM), the current DACs ($I_{DAC,a,c}$) for biphasic stimulation, and the charge balancing circuits. Each stimulation channel is equipped with passive charge balancing using a HV switch for instantaneous charge compensation. Additionally, channel 01 and 05 provide active CB that corrects the charges of the stimuli, and therefore, is advantageous in chronic long-term implantation. The latter is the topic of chapter 5. The stimulator front-end is based on the principle of a regulated input cascode current mirror. Thus, in addition to an increased output voltage compliance, which allows for very low output voltage operation modes, an improved mirroring accuracy, and an increased output resistance were achieved. For optimal flexibility in pulse shape variations and stimulus amplitudes, the proposed current mirror was designed as a 8-bit current DAC with additional adjustable current biasing. The circuit design, loop analysis and measurement results are presented and discussed in this section.

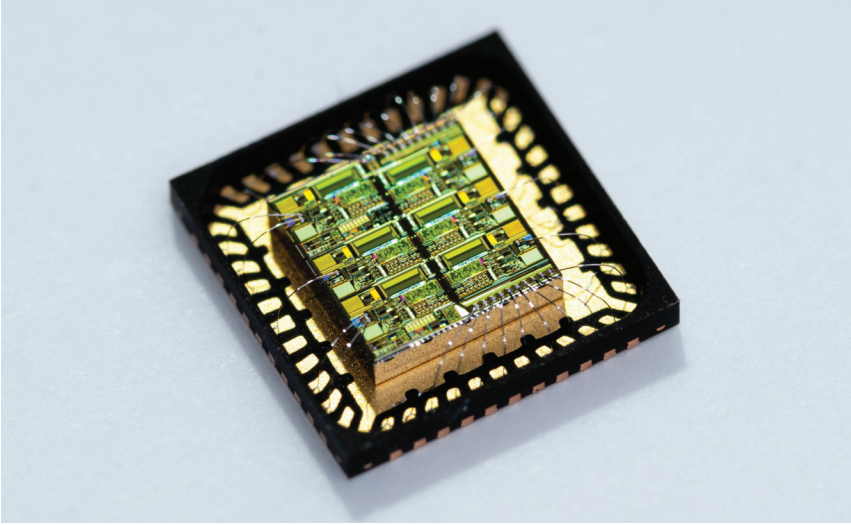


Figure 4.4.: Chip photo of the biphasic six channel current stimulator front-end.

[3]The work presented in this section comprises exclusively the analog part of the biphasic stimulator front-end ($I_{DAC,a,c}$), to which the author has contributed. The current mirror concept and NMOS $I_{DAC,c}$ design were investigated and implemented by Armin Taschwer. The author thereby supported Armin Taschwer by design considerations and improvements concerning the switching options. The author implemented the PMOS $I_{DAC,a}$ in accordance to the NMOS part and verified the performance of both current DACs by simulations and system analysis for the different settings. Further, the author made a considerable contribution to the layout of the current DACs, as well as the top-level layout of the analog stimulator front-end. The content of this sections is partially published in [61] (©2018, IEEE) and [62].

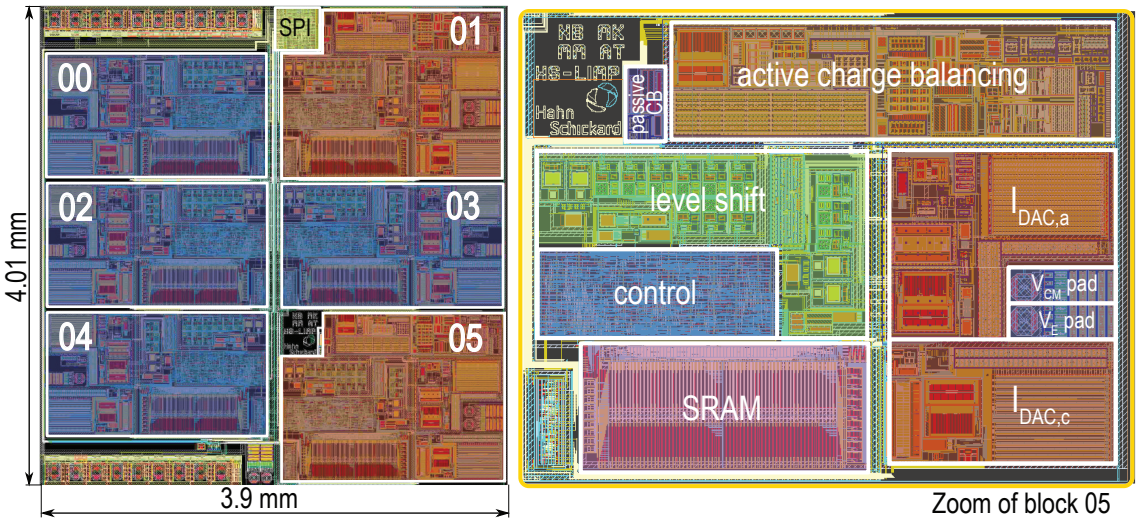


Figure 4.5.: Layout organization of the six channel current stimulator chip. Labels adjusted from [61] (©2018, IEEE).

4.3.1. Regulated Input Cascode Current Mirror

The topology of a regulated input cascode current mirror for the cathodic (NMOS) current mirror side is shown in Fig. 4.6(a). In a simple well matched current mirror, the accuracy of the mirroring ratio between the reference current I_{ref} and output current depends on their drain to source voltage differences. Therefore, a regulated input current mirror increases the accuracy by controlling the drain of the reference transistor M_1 to match the drain of the mirror transistor M_2 of the output branch [65–67]. The proposed architecture additionally introduces the cascode transistor M_4 biased by the input gate voltage $V_{\mathrm{G1,2}}$. In this way, the drain of M_2 is held low enough to force M_2, and therefore also M_1, to operate in triode region under all conditions, which minimizes their voltage headroom (V_{head}). A further benefit, due to the operation in triode region is that the random current error of the circuit is reduced, since V_{th} variations have a reduced impact in triode region [65]. In the working condition where M_1 and M_2 are both in triode region and V_{E} stays above the saturation point of M_4

$$r_{\mathrm{out}} \approx A \cdot g_{\mathrm{m4}} \cdot r_{\mathrm{ds4}} \cdot r_{\mathrm{ds2,triode}} \ . \tag{4.1}$$

Beside the mentioned advantages of a smaller voltage headroom and a reduced impact of threshold variations, r_{out} looses r_{ds2} in saturation, compared to a simple regulated input current mirror [66, 67]. However, the effect is eased by the multiplication with the additional intrinsic gain of M_4. Finally, the difference in r_{out} depends on the actual implementation and settings of the current mirror. The value of r_{out} might be larger or comparable to the one of a simple regulated input current mirror. Once M_4 enters the triode region, the output resistance will fall as g_{m4} and r_{ds4} are both decreasing. However, since A is large, r_{out} is maintained at an acceptable high

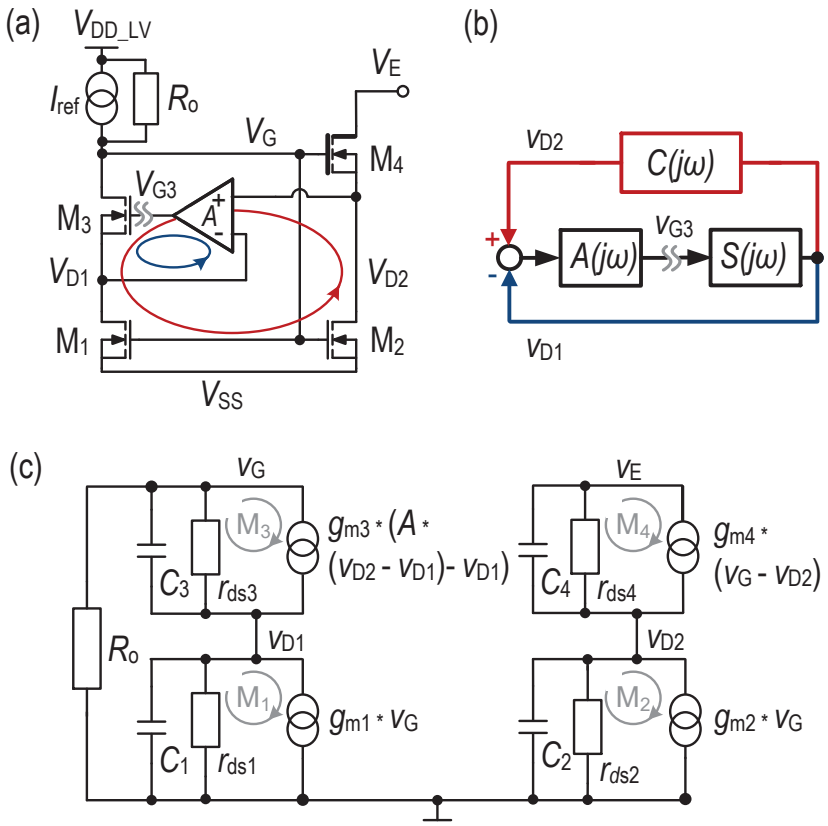


Figure 4.6.: (a) Topology of the NMOS regulated input cascode current mirror. (b) Open loop control representation for loop gain calculations. (c) Small signal equivalent circuit.

value over the whole output voltage range [65]. Results of the output resistance of the implemented current DAC for different settings are presented in sec. 4.3.3.

The control circuitry of the regulated input cascode current mirror uses a differential input operational amplifier (OPA) with gain A to compare the drain voltages of M_1 and M_2. The output of the OPA then steers the input cascode transistor M_3 to match the drain of the reference transistor M_1 accordingly. Compared to a regulated output cascode architecture [4, 6] the power requirement of the OPA is reduced, since only one gain-stage at the input cascode is controlled. The amplifier consumes 140 nA only. Its design makes use of a low-power folded-cascode gain stage with PMOS input. In this way, correct operation is also guaranteed for voltage input levels close to ground.

Having a closer look at the control circuitry, two control paths can be distinguished [68]: one with negative feedback via the OPA and M_3 and the other with positive feedback via the OPA, M_3, M_1 and M_2. In Fig. 4.6(b) the circuit is illustrated in a standard control representation, where $A(j\omega)$ is the gain of the OPA, $S(j\omega)$ the gain of M_3 that is implemented as a source follower and $C(j\omega)$ the voltage gain

due to the basic current mirror components M_1 and M_2. The overall closed loop characteristic of the current DAC yields

$$r_{\text{out}} = \frac{v_{\text{out}}}{i_{\text{out}}} = \frac{g_{\text{m4}} \cdot r_{\text{ds4}} \cdot r_{\text{ds2,triode}} \cdot A(j\omega) \cdot S(j\omega)}{1 - A(j\omega) \cdot S(j\omega) \cdot (C(j\omega) - 1)} \,. \tag{4.2}$$

From the denominator of Eq. (4.2), and also from the loop representation in Fig. 4.6(b), the system is stable if the loop gain

$$A_{\text{LG}} = |A(j\omega) \cdot S(j\omega) \cdot (C(j\omega) - 1)| < 1 \,, \tag{4.3}$$

holds, which is the open loop gain stability criterion for positive feedback loops. Therefore, it is important as a first step to show that the loop is stable at low frequencies, before examining the loop stability in the frequency domain. The exact calculation of the source follower gain at low frequencies $S(j\omega = 0)$ using small signal analysis is given in sec. A.1. Under the assumption that $S(j\omega = 0)$ equals to around 1 and $A(j\omega = 0)$ is chosen sufficiently high, it can be concluded that the system is stable at low frequencies if

$$C(j\omega = 0) < 1 \,. \tag{4.4}$$

$C(j\omega = 0)$ is extracted by small signal analyses of the circuit

$$C(j\omega = 0) = \frac{v_{\text{D2}}}{v_{\text{D1}}} = \frac{v_{\text{D2}}}{v_{\text{G}}} \cdot \frac{v_{\text{G}}}{v_{\text{D1}}} \,. \tag{4.5}$$

The contribution of the first term is found by looking at the loop of transistor M_2 of the small signal equivalent circuit in Fig. 4.6(c) and results to

$$\frac{v_{\text{D2}}}{v_{\text{G}}} = -r_{\text{ds2}} \cdot g_{\text{m2}} \,. \tag{4.6}$$

The contribution of the second term is derived by equalizing the current through R_{o} with the current through transistor M_1

$$\frac{-v_{\text{G}}}{R_{\text{o}}} = g_{\text{m1}} \cdot v_{\text{G}} + \frac{v_{\text{D1}}}{r_{\text{ds1}}} \,, \tag{4.7}$$

where R_{o} is the output resistance of the reference source I_{ref}. Rearranging Eq. (4.7) yields to

$$\frac{v_{\text{G}}}{v_{\text{D1}}} = \frac{-1}{r_{\text{ds1}} \cdot (g_{\text{m1}} + \frac{1}{R_{\text{o}}})} \,. \tag{4.8}$$

Finally, $C(j\omega = 0)$ results to

$$C(j\omega = 0) = \frac{g_{\text{m2}} \cdot r_{\text{ds2}}}{g_{\text{m1}} \cdot r_{\text{ds1}} + \frac{r_{\text{ds1}}}{R_{\text{o}}}} \,. \tag{4.9}$$

Considering good matching between the intrinsic gain ($g_{\mathrm{m}} \cdot r_{\mathrm{ds}}$) of M_1 and M_2 the requirement of Eq. (4.4) is fulfilled due to the small contribution of $r_{\mathrm{ds1}}/R_{\mathrm{o}}$ in the denominator of Eq. (4.9). This also holds for different current mirror ratios, since in the linear region $r_{\mathrm{ds1}\,1,2}$ and $g_{\mathrm{m1,2}}$ are inversely proportional to W/L. Consequently, the circuit is stable at low frequencies despite the loop contribution of the positive feedback path. However, the frequency response of the control circuitry is not considered so far. Therefore, simulations that take the exact values of all circuit components for all different stimulator settings are carried out. The results of the specific overall loop behavior over the relevant frequency range is presented in sec. 4.3.3.

4.3.2. Current DAC Design and Implementation

The architectures of the cathodic and anodic current sources are identical, however, inverted considering transistor types, as shown in Fig. 4.7. Both current sources were designed as a 8-bit current DAC. It is basically transistor M_2 of Fig. 4.6 that consists of multiple binary-dimensioned and switchable transistors. For further output current flexibility, each DAC is biased by a 3-bit adjustable reference current I_{ref} of 1 µA, 2 µA, 4 µA and 10 µA plus a doubling option for each, to set the coarse amplitude range. The smallest current mirror ratio is 1:2, thus starting with a LSB of 2 µA. The feasible maximum stimulus amplitudes per range result to 0.5 mA, 1 mA, 2 mA and 5 mA, and with doubling option to even 10 mA. Additionally, a fixed bias current I_{bias} of 100 nA is added to I_{ref} to allow a fast start up condition. This biasing current will later be used to introduce an error current for offset compensation by active charge balancing.

Each transistor M_2^i of the current DAC is switchable by a series transistor S_{en}^i. Additionally, at the high-current (HC) amplitude ranges (I_{ref} of 4 µA and 10 µA), the dimensions of M_1 and M_2^i are adjusted by parallel transistor paths via $M_{1\mathrm{HC}}$ and $M_{2\mathrm{HC}}^i$ and their switches respectively. In a first prototype the cascode transistor M_4 was also switchable and binary coded to keep the working point condition more or less constant. However, switching events in the output branch cause over and undershoots in the output current and electrode voltage. These over and undershoots are mainly caused by the charge induced due to the parasitic gate-drain capacitance C_{gd4} of the switched cascode transistors M_4, since these charges are directly drawn from the electrode-tissue interface. The amplitude and duration of the over and undershoots are depended on the size of C_{gd4}, which varies with the chosen bit number of M_4. Indeed, the duration is very short and the charge that is injected to or drawn from the tissue is negligible compared to the total amount of charge that is injected for successful stimulation. However, to avoid this effect to which the switching of M_4 contributes the most, M_4 is no longer binary coded in the second prototype and an optimized fix dimension of M_4 is taken for all settings. In this way, the stacked cascode transistor M_4 is able to reduce over and undershoots by isolating the gate-drain capacitance C_{gd2} of the switched transistors M_2 from the

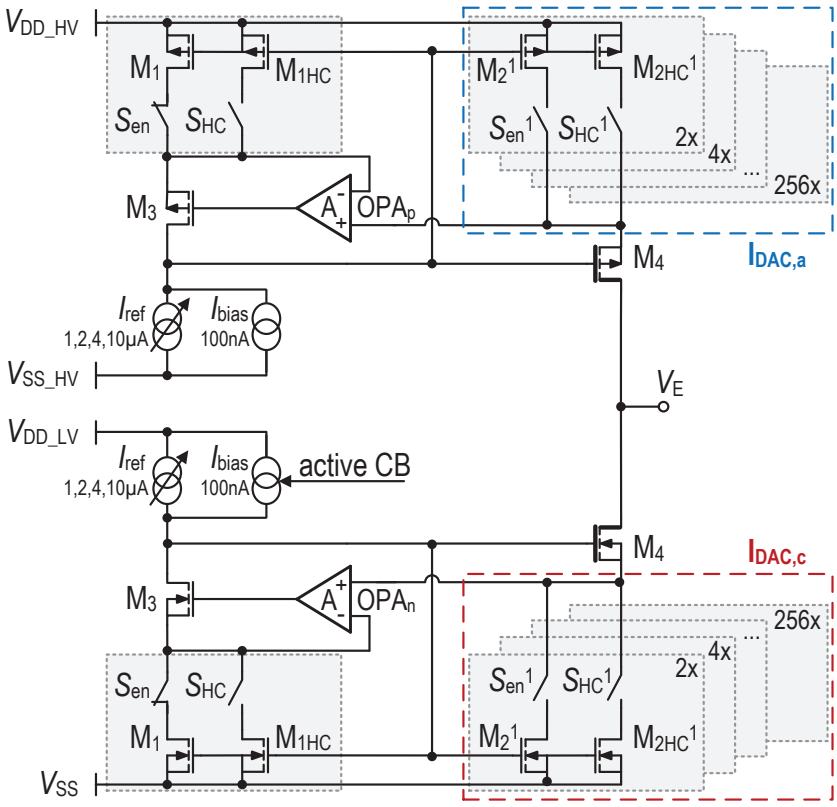


Figure 4.7.: Implementation of the cathodic ($I_{DAC,c}$) and anodic ($I_{DAC,a}$) current DACs. Reproduced and adjusted from [61].

output node. In order to further eliminate over and undershoot effects, all switches that are in the direct path of the simulation current, which are the series switches of all M_2 transistors, would have to be replaced by gate switches for M_2 instead [69].

4.3.3. Stability Considerations

Changing transistor dimensions by adjusting the HC setting according to I_{ref}, or switching between different bit settings, causes a change in the DAC's characteristics like voltage headroom, output resistance, and parasitic capacitance C_{gs2}. The latter affects the loop behavior. Therefore, these characteristic values and the loop stability must be ensured for all possible settings and the circuit must be optimized accordingly. The simulation results for V_{head}, r_{out} as defined in Eq. (4.1), and the loop characteristics are presented in Tab. 4.1. The results are listed for the LSB and full scale settings of each amplitude range for $I_{DAC,a}$ and $I_{DAC,c}$, respectively. V_{head} ranges from 30 mV in the best case to 410 mV in the worst case for $I_{DAC,c}$ and to 750 mV for $I_{DAC,a}$. The r_{out} values lie between 0.08 GΩ to 971 GΩ for $I_{DAC,a}$ and 0.24 GΩ to 3589 GΩ for $I_{DAC,c}$. In general, the performance of $I_{DAC,a}$ is slightly worse compared to $I_{DAC,c}$ due to the difference in NMOS and PMOS charge mobil-

Table 4.1.: Simulation results of the voltage headroom (V_{head}), output resistance (r_{out}) and the loop characteristics DC gain (A_{dc}), phase margin (PM) and unity gain band width (UGBW) of $I_{DAC,a}$ and $I_{DAC,c}$ respectively.

	$\mathbf{I}_{DAC,a}$					$\mathbf{I}_{DAC,c}$				
Current I_{Stim} for each range	V_{head} (mV)	r_{out} (GΩ)	A_{dc} (dB)	PM (°)	UGBW (MHz)	V_{head} (mV)	r_{out} (GΩ)	A_{dc} (dB)	PM (°)	UGBW (MHz)
LSB: 2 µA	30	686	108	37	5.33	30	2871	104	64	4.32
Full scale: 0.51 mA	50	6.9	112	42	4.01	40	1456	109	67	3.42
LSB: 4 µA	50	971	110	35	6.00	50	3589	105	62	4.79
Full scale: 1.02 mA	100	6.3	113	39	4.79	70	13.8	109	65	3.87
LSB: 8 µA	30	402	114	30	3.49	30	1290	107	59	2.80
Full scale: 2.05 mA	130	1.7	114	48	2.44	70	4.1	110	69	1.97
LSB: 20 µA	70	656	113	23	4.16	70	2424	107	55	3.32
Full scale: 5.12 mA	330	1.5	115	43	2.96	170	4.6	109	67	2.32
2x full scale: 10.24 mA	750	0.08	115	39	3.33	410	0.24	98	72	2.48

ity when using similar transistor dimensions. To achieve more similar cathodic and anodic results of V_{head} and r_{out}, the PMOS transistor width must be increased by a factor of around three. However, increasing transistor dimensions will also increase the parasitic caps, which in turn will change the loop behavior. Additionally, all anodic PMOS transistors have to be used with an increased well for HV robustness, which makes the die area of $I_{DAC,a}$ already larger than the one of $I_{DAC,c}$ and further enlargement is undesirable.

The circuit characteristic bode plot, shown in Fig. 4.8, was simulated by opening the loop at the gate of M_3. The open loop transfer functions of the $I_{DAC,a}$ and $I_{DAC,c}$ match well. Both provide two dominant poles, followed by a zero and more poles at higher frequencies, the latter however cause a difference in phase margin (PM). The first pole p_{OPA} is the output pole of the OPA. The second pole p_{CM} results from the current mirror configuration of M_1 and M_2^i. Comparing Fig. 4.8(a) and (b), it is traceable that changing from LSB to full scale shifts the second pole further to the left due to the increased parasitic capacitance C_{gs2}. Stability of the control loop was proven by a PM that lies between 59° and 69° for $I_{DAC,c}$ and between 30° and 48° for $I_{DAC,a}$. The PM of $I_{DAC,a}$ is rather small and additionally, the phase is even at a lower value before the zero dB crossing. Therefore, further optimization to increase the PM and to push the transfer function towards a one pole system is required. However, increasing the output capacitance C_{OPA} of the OPA_a will not be efficient enough, like illustrated in Fig. 4.9 by the dotted blue lines. A more promising approach is to split the two dominant poles by introducing an additional capacitance C_{gd3} between the gate and the drain of M_3, as also shown in Fig. 4.9. This is just a suggestion for future work, further investigations are needed.

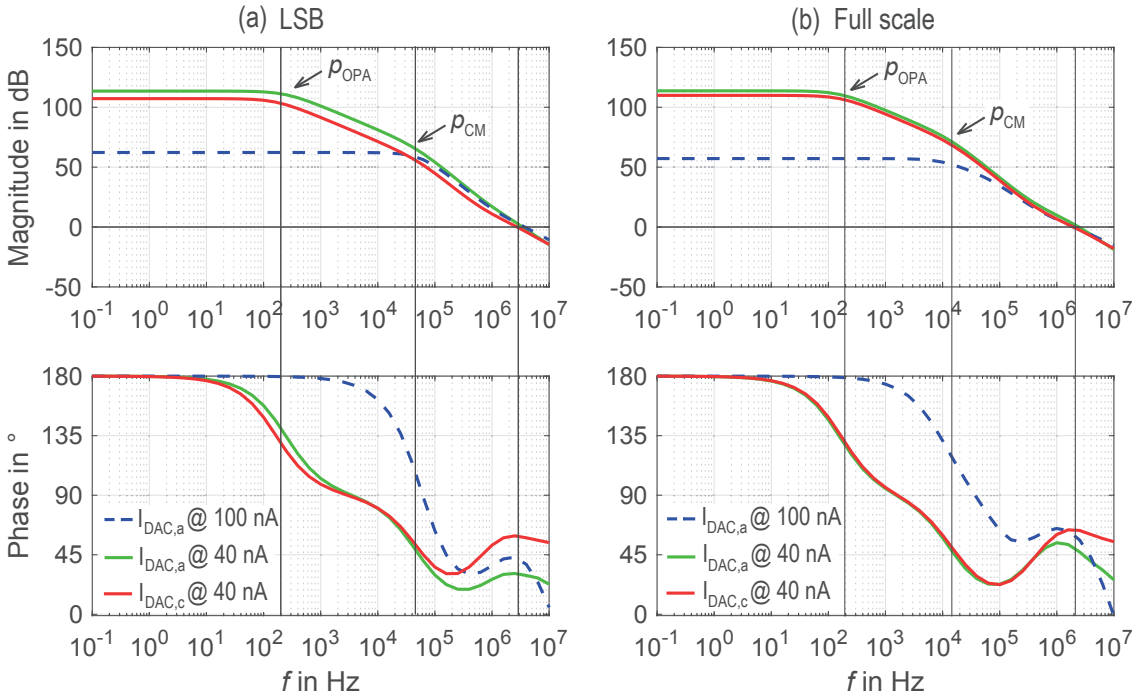


Figure 4.8.: Simulated bode plot of the open loop gain and phase of the cathodic ($I_{DAC,c}$) and anodic ($I_{DAC,a}$) current DAC controls, (a) shown for the worst case setting concerning PM at LSB: 8 µA, and (b) at full scale: 2.05 mA.

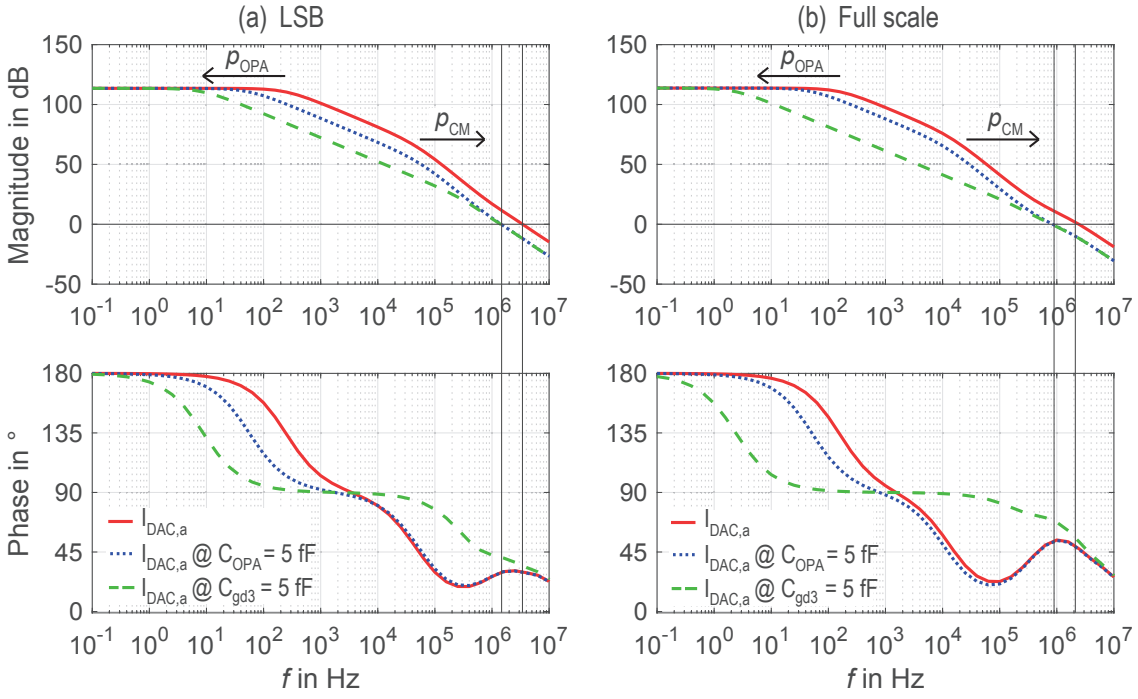


Figure 4.9.: Suggestion for PM optimization of $I_{DAC,a}$ for future work, (a) shown for the worst case setting concerning PM at LSB: 8 µA, and (b) at full scale: 2.05 mA.

4.3.4. Measurement Results

During measurements[4], the supply voltages for the four rails V_{SS}, V_{DD_LV}, V_{SS_HV}, and V_{DD_HV} were applied externally. The voltage headroom of the current DACs were determined by measuring the output current at a varying output voltage. The measurement results are visualized in Fig. 4.10 for the maximum amplitudes of the four current ranges, including the full scale option: 0.5 mA, 1 mA, 2 mA, 5 mA and 10 mA. The headroom voltages are listed in Tab. 4.2. For the 1 mA range of $I_{DAC,c}$ is roughly 90 mV and around 250 mV for $I_{DAC,a}$. The results of $I_{DAC,c}$ show only small deviations compared to the simulation results shown in Tab. 4.1. However, a mistake in the $I_{DAC,a}$ layout part was found, that resulted in a worse performance compared to the simulation results. It concerns the current biasing of the OPA_p that was implemented too high, 100 nA instead of the supposed 20 nA to 40 nA. The higher current in the OPA_p output branch reduces its output swing. Thus, the OPA_p is not working properly for output voltages close to the rails. This does not only influence V_{head} but also changes the loop DC gain (A_{dc}). However, during chip measurements an erroneous output current, can be adjusted manually due to its various setting options.

The measured worst case integral and differential nonlinearity (INL and DNL) results of the current DACs are shown in Fig. 4.11. The DNL is less than ±0.84 LSB and the INL is less than ±3.5 LSB, considering the 5 mA range. The increased bias

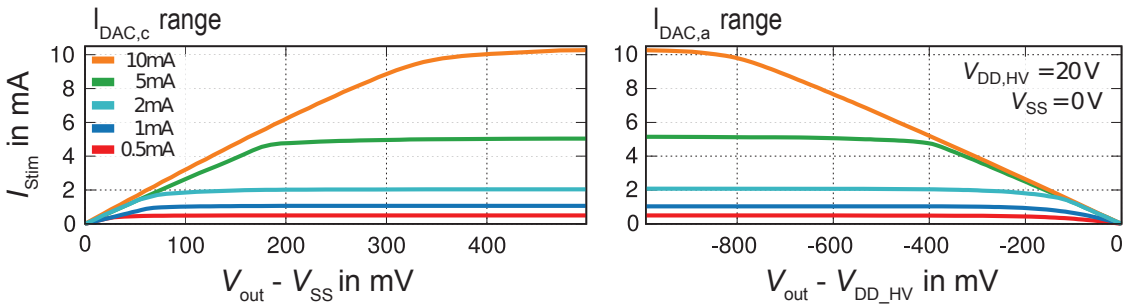


Figure 4.10.: Measured output current characteristic, for $I_{DAC,c}$ and $I_{DAC,a}$ [61] (©2018, IEEE).

Table 4.2.: Measured voltage headroom V_{head} for $I_{DAC,c}$ and $I_{DAC,a}$.

Current Range	mA	0.5	1	2	5	10
V_{head} of $I_{DAC,c}$	mV	50	90	120	250	480
V_{head} of $I_{DAC,a}$	mV	150	250	300	650	950

[4]The chip characterization and measurements were carried out by Armin Taschwer and supported by Manuel Köhler. The results have been partly published in [61] (©2018, IEEE).

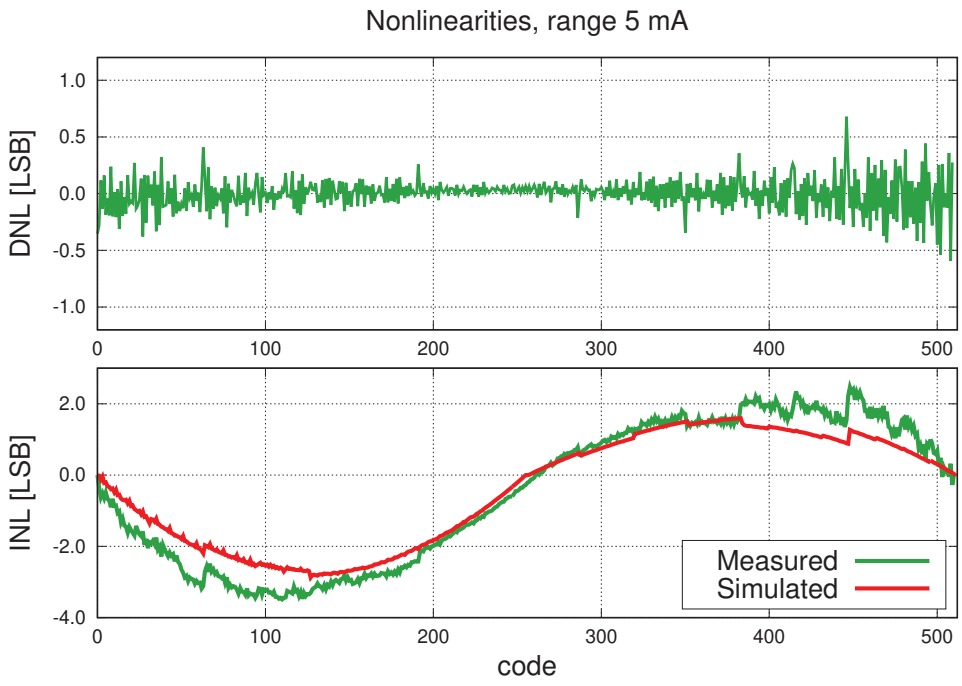


Figure 4.11.: Static performance measurement of DNL and INL for the 5 mA range.

current of the 5 mA range drives the gate voltages of M_3 closer to the rails and results in a worse linearity. OPA_p is affected more than OPA_n. Additionally, with a higher output current more nonlinearity origins from IR-drops on the supply wires of the current DACs.

To demonstrate the capability of the arbitrary waveform generation, the current DACs were programmed to perform biphasic pulses from rectangular to sinusoidal forms. The current waveforms shown in Fig. 4.12(a-d), were measured across a 1.8 kΩ resistance. In (a) a rectangular pulse shape with cathodic-first stimulus and inter-pulse delay is chosen. The falling and rising time constants were extracted and are 0.8 µs for the 2 mA range. A ramp function is shown in (b). In (c) an asymmetric signal burst is demonstrated, starting with a steep rise and smooth linear fall of the cathodic stimulus (also possible as exponentially decaying shape), followed by a sinusoidal anodic phase. As another example, (d) shows an amplitude modulated sinusoidal function that might be used for HF blocking techniques. Further, the system was tested in an in-vitro environment with platinum electrodes of different sizes in phosphate-buffered saline solution, illustrated in Fig. 4.13. Here, an exponentially decaying cathodic stimulus followed by an exponentially decaying anodic pulse was applied across one of the smaller electrodes no. 9. The electrode impedance necessitates a HV compliance of more than ±8 V at 1 mA stimulus amplitude. The stimulus was manually charge balanced by several programming iterations of the $I_{DAC,a,c}$ settings.

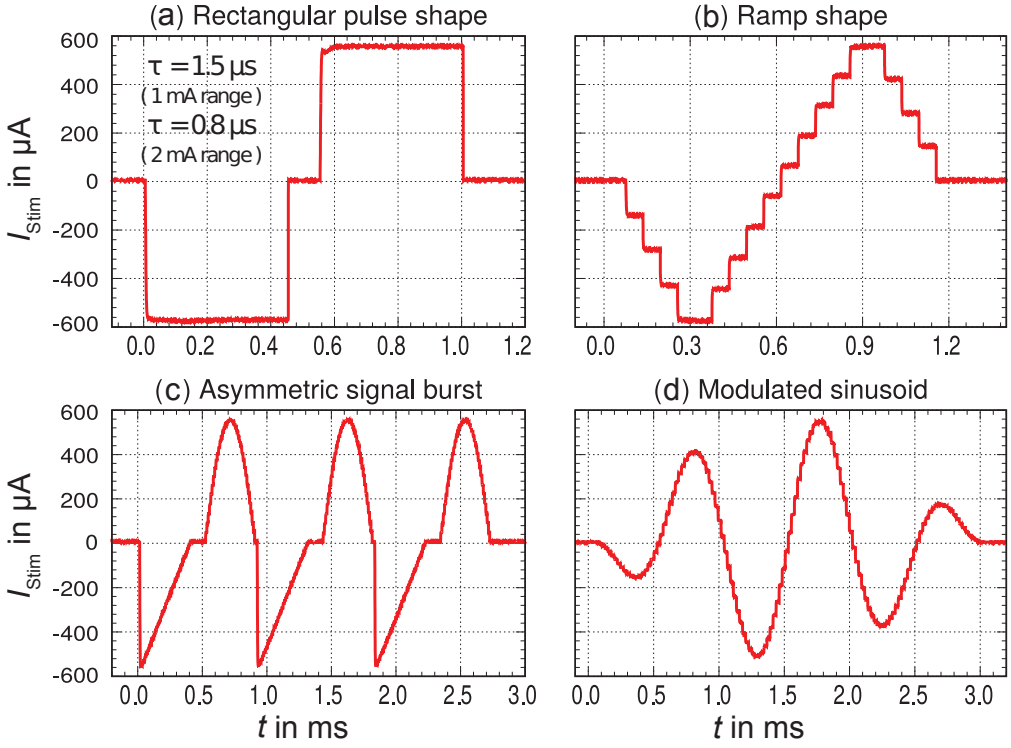


Figure 4.12.: Arbitrary waveform generation measured for (a) rectangular pulse with cathodic-first stimulus and inter-pulse delay, (b) ramp function, (c) asymmetric signal burst, and (d) amplitude-modulated sinusoid [61] (©2018, IEEE).

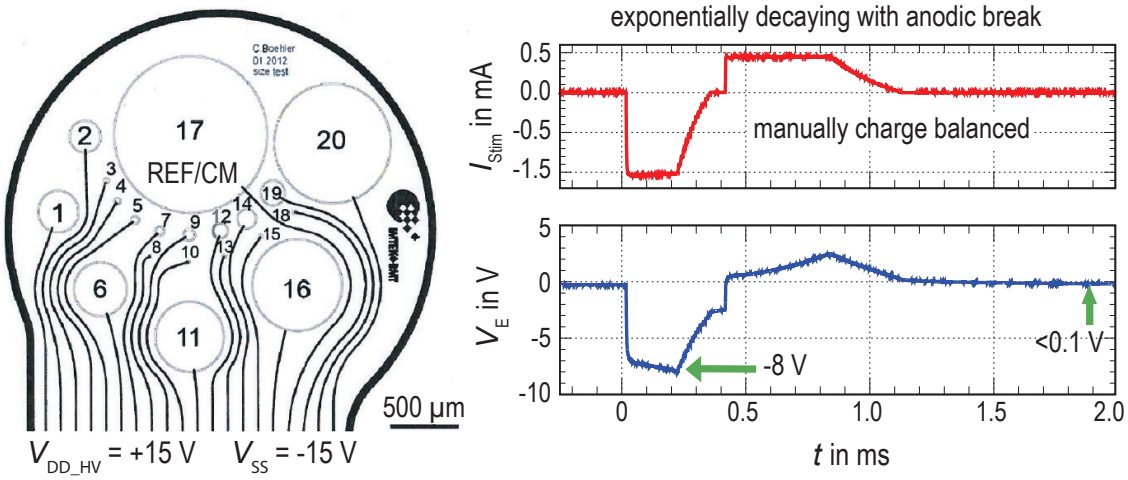


Figure 4.13.: In-vitro measurement results for an exponentially decaying stimulus via electrode 9. Adapted from [61] (©2018, IEEE).

4.3.5. Comparison to State-of-the-Art Stimulator Front-Ends

The presented stimulator front-end, is compared against similar solutions [4, 6, 57, 70] in Tab. 4.3. The system is manufactured in a 0.35 µm CMOS process with HV options. The achieved HV compliance range of 3.3 V to 49 V is outstanding. The low voltage headroom of 90 mV at 1 mA allows the best use of the full HV compliance, compared against [4, 6, 57, 70]. The overall static power consumption P_{stat} of the stimulator, excluding the on chip charge balancers, is only 20.8 µW at a 3.3 V supply and less than doubled 41 µW at a 49 V supply.

Finding an optimal stimulus pulse shape is still a wide research topic [38]. Additionally, methods for selective stimulation like high-frequency (HF) block, where square shaped bipolar stimuli excite the nerve and secondary HF sinusoidal stimuli block the nerve at an adjacent site, require flexibility of the stimulator in arbitrary waveform generation. Recently published current-controlled stimulators [4, 6, 57, 70] show limited flexibility in either dynamic output current range or arbitrary waveform generation. Therefore, the proposed current DACs provide freely and independently programmable current pulse shapes with 8-bit amplitude resolution. Further, the size of electrodes comprises a large specification range, and consequently, the stimulation current amplitudes need to be adaptive. The ability of controlled arbitrary waveform generation with current amplitudes from ±2 µA to ±10 mA, is the highest reported. Providing current amplitudes of up to ±10 mA allows the use of the stimulator for a broader range of applications; even Transcutaneous Electrical Nerve Stimulation is in the scope [61].

Table 4.3.: Comparison of the stimulator performance to the state-of-the-art. Adapted from [61].

Reference		TBioCAS 2014 [57]	TBioCAS 2017 [70]	JSSC 2013 [6]	JSSC 2012 [4]	**This work** 2018 [61]
CMOS process	µm	0.35	0.18	0.5	0.35	0.35
$V_{\text{DD\_HV}}$	V	15	3.3	2.5 to 4.6	5 to 20	**3.3 to 49**
$P_{\text{stat,min}}$	µW	30	N/A	35	209	**21 to 41**
$I_{\text{Stim,min}}$	µA	35	N/A	80	4	**2**
$I_{\text{Stim,max}}$	mA	1	0.25	2.5	1	**10**
Resolution	bit	5	8	5	5	**8**
V_{head}	mV	800	240	150	300	**90**

4.4. High-Voltage Switch

Important components of the interface between stimulator and charge balancer are the switches, shown in the system overview of Fig. 4.2. The switches S_1 and S_2 are used to ensure that the stimulation and the charge balancing process do not overlap with each other. The switch S_P represents passive CB by electrode shortening via its on-resistance. Due to the stimulation current requirements and electrode impedances the overall system, including the switches, must provide HV compliance. A general lack of HV switches was mentioned in [5, 34, 40, 71], "(...) since even in a dedicated HV process transistors only withstand high drain-source, but not high gate-source voltages, which are required by a transmission gate switch!" [40]. This chapter presents a solution for HV switches elaborated in a 0.35 µm CMOS technology with HV option.

4.4.1. Design Considerations

The HV switch mainly consists of the switching transistor M_{sw} and a HV logic level shifter, shown in Fig. 4.14. The switching architecture is the same for all implemented HV switches. However, depended on the purpose, the switches differ in their on-resistance. Switch S_1 and S_2 of Fig. 4.2 are connected to a gate of an input transistors of the monitoring circuits. Thus, they are not part of a current path and their on-resistance is not crucial. Therefore, it is appropriate to optimize these kind of switches for low area. However, for S_P the main focus of attention must be on its on-resistance, since it is crucial for successful charge compensation. The time to conduct a compensation current is limited. Therefore, S_P must provide a low resistance after, but a high one during stimulation. However, the on-resistance should not be too small to avoid compensation current amplitudes that might trigger unwanted action potentials. The on-resistance of the proposed switch was chosen in the kilo-ohm range by an adequate dimensioning of the main switching transistor M_{sw} and its applied gate-source voltage ΔV_{GS}.

The input and output terminals T_{in} and T_{out} of M_{sw} may be applied to HV. Additionally, it is not known in advance whether T_{in} or T_{out} is larger. Therefore, M_{sw} is a symmetrical HV PMOS transistor, using a passive winner-takes-all method for the bulk connection. The latte consists of two HV PMOS transistors M_l and M_r and two Schottky diodes, in the shown arrangement of Fig. 4.14. Dependent on the terminal voltages, either M_l or M_r is conducting and connects the middle node N_m to the larger potential, which then defines the source of M_{sw}. Additionally, all bulk terminals must be connected to the highest potential node N_m. However, the threshold voltage of the chosen HV $M_{l,r}$ transistors is quite high, around 1 V. Therefore, Schottky diodes with a forward voltage of around 120 mV only were included to support the winner-takes-all principle. Thus, the diodes avoid current through the parasitic transistor diodes, as long as the voltage difference between the two

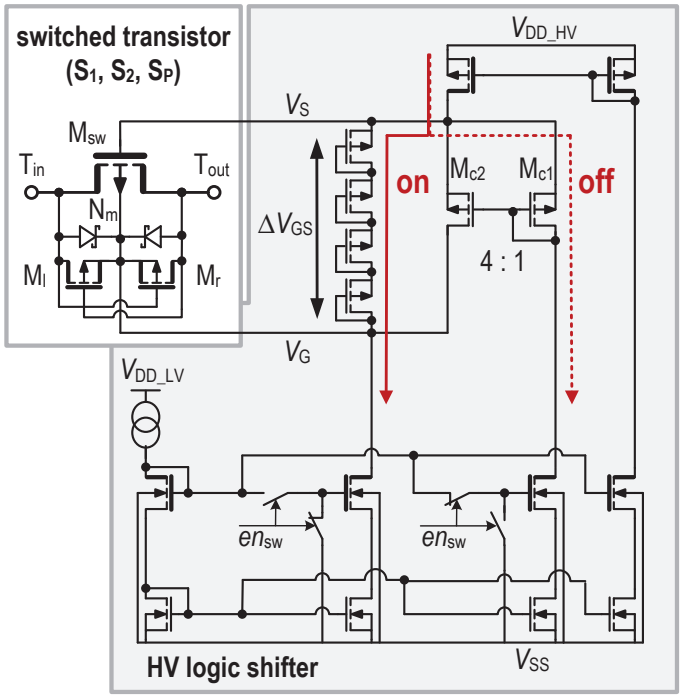


Figure 4.14.: Implementation of the HV switch, including the HV logic shifter. The bold terminals indicate the HV protection of the used transistor types.

terminals is smaller than the threshold voltage of $M_{l,r}$. Once M_l or M_r opens, the diodes are shorted and N_m follows the highest potential without any voltage drop due to the diodes.

To open M_{sw}, a sufficient ΔV_{GS} is needed. However, in the system's quad rail concept, all digital signals are within the $\triangle V_{LV}$ domain with a swing of V_{DD_LV}. Therefore, a HV logic shifter is required to shift the LV digital control signal en_{sw} into the respective HV domain. In the 'on' condition, a current of e.g. 10 nA is directed through a series of floating diode-connected transistors, providing a sufficient ΔV_{GS} to open M_{sw}. In the 'off' state, the same 10 nA are being directed through a second branch via M_{c1}, actively pulling V_G toward V_S due to the parallel current mirror transistor M_{c2}, thus closing M_{sw}.

The restricting operation voltage of the presented switch architecture in the used HV CMOS technology is the maximum allowed gate-drain voltage of M_{sw} in the 'off' condition. Thus, the voltage difference between T_{in} and T_{out} is restricted to a maximum of 20 V. However, during stimulation, the switches are used in a way that one terminal is always connected to V_{CM} and the other to V_E. Assuming that

$$V_{CM} = (V_{DD\_HV} + V_{SS})/2 \tag{4.10}$$

and V_E swings towards the supply values, the switch can be used for a maximum allowed supply V_{DD_HV} of up to 40 V. The minimum possible supply results from the

Table 4.4.: Results of a Gaussian distributed Monte Carlo simulation with 200 runs at 20°C and a 40 V supply.

	ΔV_{GS} in V			$\mathbf{S_P}$: min. R_{on} in kΩ			$\mathbf{S_{1,2}}$: min. R_{on} in kΩ		
I_{bias}	20 nA	10 nA	5 nA	20 nA	10 nA	5 nA	20 nA	10 nA	5 nA
typical	3.41	3.18	2.96	2.43	2.22	2.34	4.41	4.06	4.30
mean	3.40	3.17	2.95	2.63	2.69	2.59	4.80	4.99	4.85
σ	0.12	0.12	0.12	0.50	0.63	0.54	0.80	1.09	0.96
S_P:	t_{delay} in µs			t_{rise} in µs			t_{fall} in µs		
I_{bias}	20 nA	10 nA	5 nA	20 nA	10 nA	5 nA	20 nA	10 nA	5 nA
typical	15.1	29.4	56.8	58.0	116.6	236.4	31.1	52.5	108.1
mean	15.1	29.3	57.6	57.8	116.6	235.5	31.0	53.0	105.5
σ	0.8	2.0	4.6	2.5	7.1	17.1	3.3	6.7	13.6
$S_{1,2}$:	t_{delay} in µs			t_{rise} in µs			t_{fall} in µs		
I_{bias}	20 nA	10 nA	5 nA	20 nA	10 nA	5 nA	20 nA	10 nA	5 nA
typical	9.0	17.2	33.9	34.9	70.1	141.3	18.4	31.3	64.3
mean	9.1	17.2	33.7	34.7	70.1	141.5	22.5	31.4	65.0
σ	0.4	1.1	2.6	1.4	4.1	10.1	1.9	3.9	9.4

sum of the needed ΔV_{GS} to open M_{sw} and the voltage drop of the current mirrors. V_{DD_HV} of 5.8 V is the smallest supply voltage for which the switch's behavior and the on-resistance are unchanged. Nevertheless, the switch works at supply voltages down to V_{DD_LV}, however, with a slowly increasing on-resistance.

4.4.2. Simulation and Measurement Results

The performance of switch S_P and $S_{1,2}$ was characterized at different biasing currents of 20 nA, 10 nA and 5 nA for mismatch and process variation by Gaussian distributed Monte Carlo (MC) simulations. The simulations were performed with 200 runs at laboratory temperature of 20°C and a 40 V supply. In the off-state, where ΔV_{GS} of M_{sw} is shorted, simulation results of both switches, $S_{1,2}$ and S_P, proved a high off-resistance larger than 0.2 GΩ. MC simulation results of the on-state, when ΔV_{GS} is sufficiently large to open M_{sw}, are listed in Tab. 4.4.

For illustration, the simulation results of both switches at a biasing current of 10 nA are depicted in Fig. 4.15, (a) showing R_{on}, and (b) the transient signal behavior.

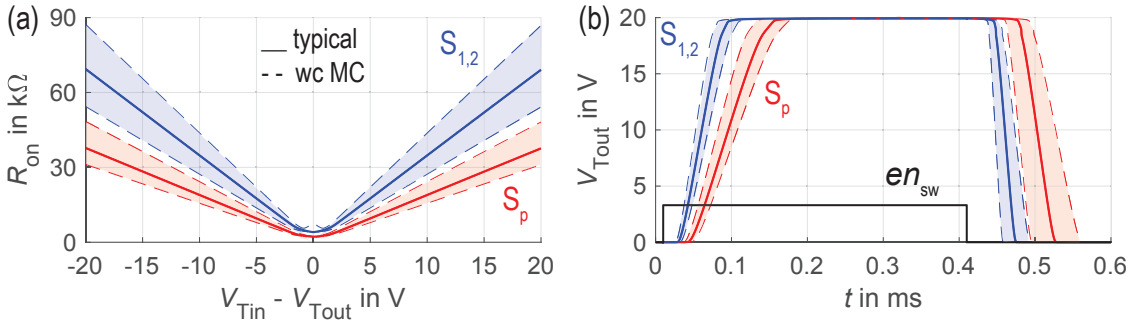


Figure 4.15.: (a) On-resistance simulated for the HV switch $S_{1,2}$ and S_P at 40 V supply and 10 nA current biasing, including the worst case Monte Carlo results. (b) Transient simulation results showing the slope to open and close $S_{1,2}$ and S_P.

The worst case MC results are additionally included. The R_{on} curve is almost flat within the linear range of M_{sw}

$$|V_{Tin} - V_{Tout}| < \Delta V_{GS} - V_{th} \approx 2\,V \tag{4.11}$$

providing a constant resistance. However, once the linear range is exceeded, the current through M_{sw} is limited by its drain current in saturation. Thus, the on-resistances of S_P and $S_{1,2}$ increase with increasing differential voltage between T_{in} and T_{out}. Comparing the on-resistance of S_P and $S_{1,2}$, the minimum on-resistance of $S_{1,2}$ is almost twice the one of S_P (Tab. 4.4). This is due to their difference in transistor dimensions of M_{sw}, with W/L of 110 µm/8 µm for S_P and 60 µm/8 µm for $S_{1,2}$. The total die area is 0.019 mm^2 for S_P and 0.014 mm^2 for $S_{1,2}$.

The transient simulation behavior of both switches, and for a maximum change in voltage with respect to V_{CM}, is shown in Fig. 4.15(b). Once the enable signal en_{sw} is high, the output voltage starts following the input voltage. However, due to the large transistor dimensions, large parasitic capacitors are created that need time to be charged (t_{rise}) and discharged (t_{fall}). Additionally, a time delay (t_{delay}) is encountered before the charging or discharging starts, which is the time needed to built up ΔV_{GS}. The smaller the biasing current of the HV switch, the larger becomes t_{delay}, t_{rise}, and t_{fall}, see Tab. 4.4. The time t_{fall}, is improved compared to t_{rise} due to the current mirror ratio of M_{c1} and M_{c2} in Fig. 4.14, which increases the current that is available for discharging the gate-source capacitor of M_{sw}. The switch $S_{1,2}$ is about twice as fast as the switch S_P, since the transistor's dimension, and thus, also its parasitic capacitance are smaller. Especially in the case of passive CB, the time to open and close S_P is of importance and must be considered in the timing diagram (Fig. 4.2). Therefore, for the application of passive charge balancing, the operation of S_P at a 20 nA biasing current is recommended.

Further, simulation and measurement results are compared for $S_{1,2}$ at different biasing currents and different minimum supply voltages in Fig. 4.16. Zoomed views of the results shown in Fig. 4.16 are provided in Fig. 4.17. The measured on-resistance

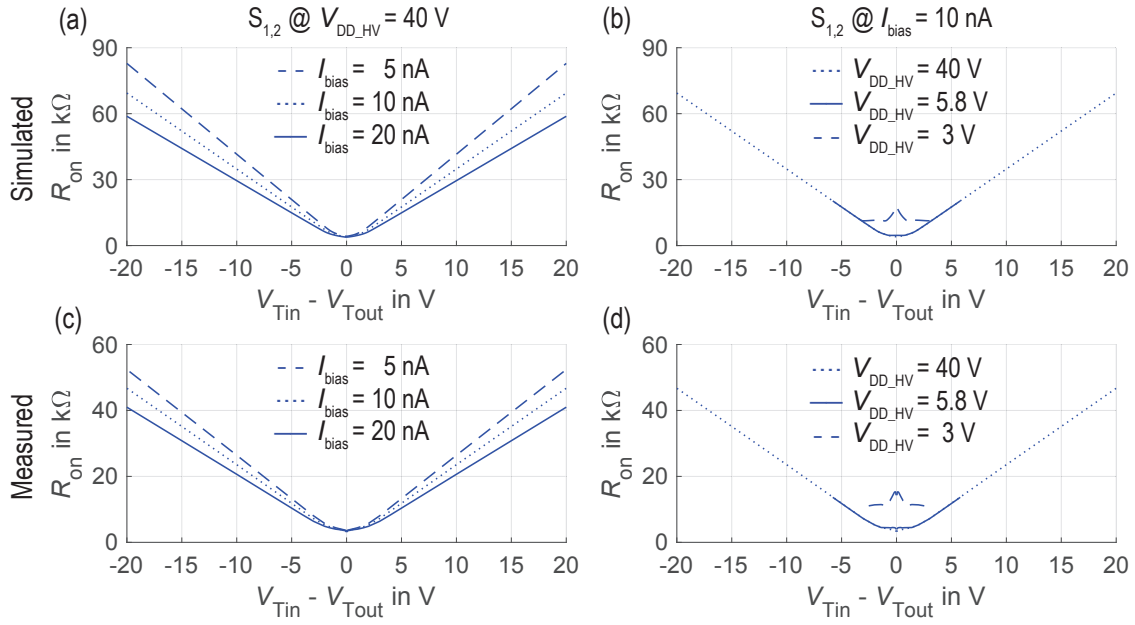


Figure 4.16.: Simulated on-resistance of $S_{1,2}$ (a) for different biasing currents I_{bias}, and (b) decreasing maximum supply $V_{\text{DD\_HV}}$. Measured on-resistance of $S_{1,2}$ for (c) different biasing currents I_{bias}, and (d) decreasing maximum supply $V_{\text{DD\_HV}}$.

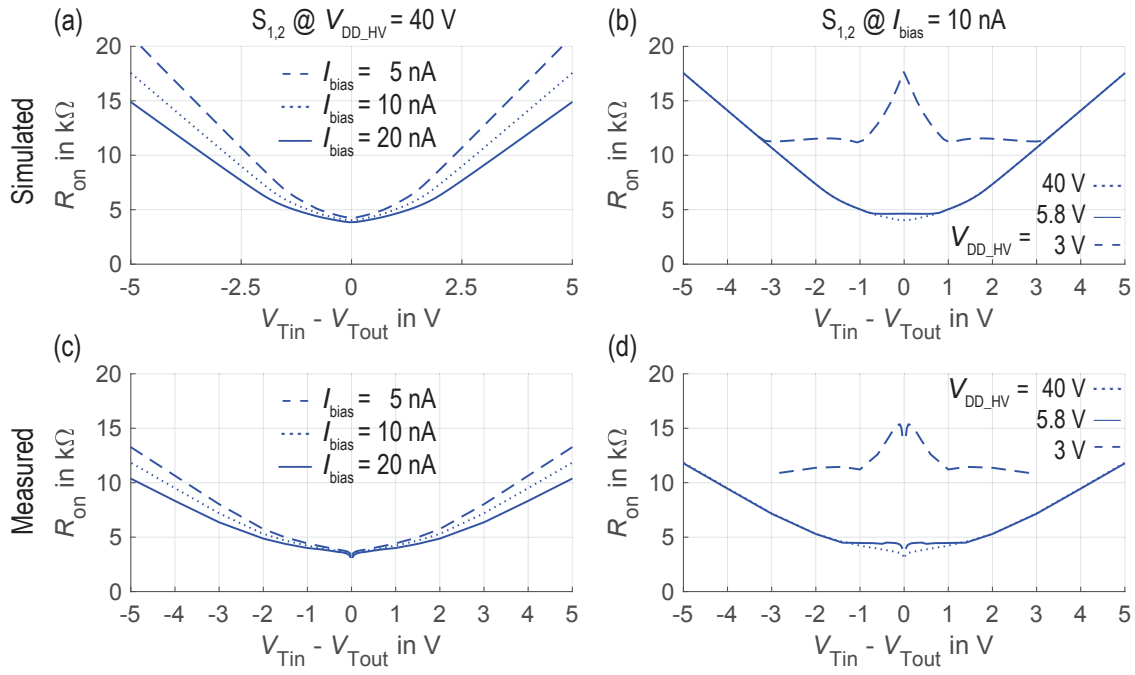


Figure 4.17.: Zoomed view of the graphs in Fig. 4.16.

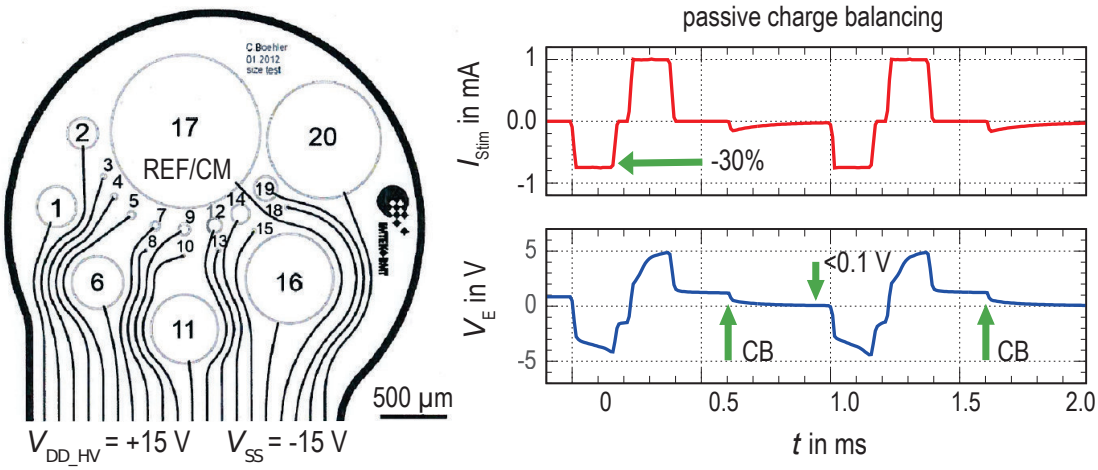


Figure 4.18.: In-vitro measurement results of passive charge balancing for a rectangular stimulus with an induced 30% cathodic mismatch, applied via electrode 20. Adapted from [61] (©2018, IEEE).

with a minimum of 3.22 kΩ is smaller than the typical value of around 4.06 kΩ that was expected by simulation, however, still lies within the two σ range. Decreasing I_{bias} also slightly decreases ΔV_{GS}, which results in a smaller drain current of M_{sw} in saturation. Thus, the slope of R_{on} becomes flatter. However, the switch works properly even at a 5 nA biasing and the power can be reduced to 0.2 µW at 40 V. The min. supply voltage $V_{\text{DD\_HV}}$ that does not cause a change in on-resistance is 5.8 V. Nevertheless, the switch can operate at smaller supply voltages, for example at a supply of 3 V. $\text{S}_{1,2}$ then still provides a minimum on-resistance in the kilo-ohm range, however, increased to 12 kΩ compared to 4.5 kΩ at a 5.8 V supply.

Passive charge balancing via S_{P} was tested in an in-vitro environment with platinum electrodes of different sizes in phosphate-buffered saline solution, illustrated in Fig. 4.18. A biphasic stimulus of ±1 mA with an intended 30% mismatch in the cathodic phase was applied via electrode no. 20. Any accumulated excess charges were subsequently compensated by passive CB and V_{E} was reduced to V_{CM}. In this way it was demonstrated, that passive CB via the HV switch S_{P}, which is incorporated in the stimulator front-end layout, is effective.

4.5. Summary

The stimulator front-end and the charge balancing systems interface at the electrode. In a system overview the overall setup was illustrated and the timing of stimulation with cause-based and consequence-based CB types was explained. First, the stimulator releases current pulses onto the electrode to excite the nervous tissue. Second, charge balancing is applied to compensate residual charges by measuring the remaining electrode voltage. According to the type of balancer, either an additional current driver compensates remaining charges, or the stimulation current sources are accessed for charge compensation. Due to the HV stimulation environment, all components must be HV compliant. Therefore, a quad-rail methodology was chosen to allow for circuit designs that are power-efficient and can adapt to different supply rails according to the needs of the application.

The implementation of the analog front-end of a power-efficient neural stimulator was presented. Its cathodic and anodic current sources for biphasic stimulation are based on a regulated input cascode current mirror principle. In this way, high accuracy, large output resistance, and little voltage overhead for an optimal output swing was achieved. An outstanding HV compliance range of 3.3 V to 49 V was realized according to the introduced quad-rail methodology. The diversity of applications demand a large range of stimulation current amplitudes. Therefore, the stimulation current sources were implemented as current DACs with 8-bit resolution each, programmable in the range of some micro-ampere up to ± 10 mA. Loop analysis at different current settings was performed and discussed. The current-controlled stimulator front-end allows for pulse shape variations, which was illustrated by chip measurements. Rectangular, sinusoidal and exponential shapes were possible, supporting e.g. selective stimulation via anodal and HF block.

To separate the proposed charge balancing circuits from the stimulator circuitry and for passive charge balancing that shorts the electrode via a switched resistor, HV compliant switches are needed. Therefore, a HV switch was implemented that provides an adequate on-resistance in the kilo-ohm range. To save power, the switch was designed to work at a biasing current as low as 5 nA. Its HV robustness of up to 40 V was proven by measurements.

5. PI-Controlled Offset Compensation

The PI-controlled Offset Compensation[5] belongs to the category of cause-based compensation methods. By means of a closed loop, the charges that remain on the electrode-tissue interface during stimulation are controlled and the cause of them is counteracted. Therefore, an offset current is supplied in the background, according to the quantity of the monitored residual electrode voltage. The balancing current is spread over time, gradually increasing or decreasing the amplitude of the cathodic stimulus. Once the cathodic stimulus is adjusted to effectively counterbalance the biphasic stimulation mismatch, a long-term quasi-static state of the electrode voltage is reached.

5.1. Conceptual Overview

A system overview of the PI-controlled Offset Compensation within the stimulation setup is given in Fig. 5.1. The PI-controlled OC consists of two main components: the controller OTA_1-$R_{\mathrm{CMOS}}C_{\mathrm{int}}$ and the current driver OTA_2. After each stimulus, V_{E} is monitored for a short time, steered by two inversely phased HV switches S_{OC}. The monitoring unit is represented by the PI controller in the shown OTA-RC configuration. The operational transconductance amplifier OTA_1 compares V_{E} to the body's quiescent potential V_{CM}, resulting in an output current I_{int} that is integrated and stored via C_{int}. Thereby, the control settings can be changed by on-chip trimming of the pseudo back-to-back CMOS resistor R_{CMOS}. The stored voltage V_{int} serves as a measure for the charge mismatch that is transformed into a background offset current I_{OC} by OTA_2. Via the switches S_{r}, V_{int} is reset before a trail starts or whenever needed. I_{OC} interfaces the biphasic stimulation DACs and forces the charges of the negative and positive current pulses to match. Here, I_{OC} is either added to or subtracted from the constant biasing current I_{bias} of $\mathrm{I}_{\mathrm{DAC,c}}$, see also Fig. 4.7. This is done in a way that makes a small current in the nano-ampere range sufficient to percentually correct I_{Stim} independent of the DAC's bit setting. In general, it is conceivable to apply I_{OC} to $\mathrm{I}_{\mathrm{DAC,a}}$ or $\mathrm{I}_{\mathrm{DAC,c}}$. In the implemented

[5]The results of this chapter have been published in [13, 63, 72] (©IEEE), in which the main author is the author of this thesis. The author performed all design, implementation and layout tasks, as well as the closed loop system analysis, simulations and chip measurements.

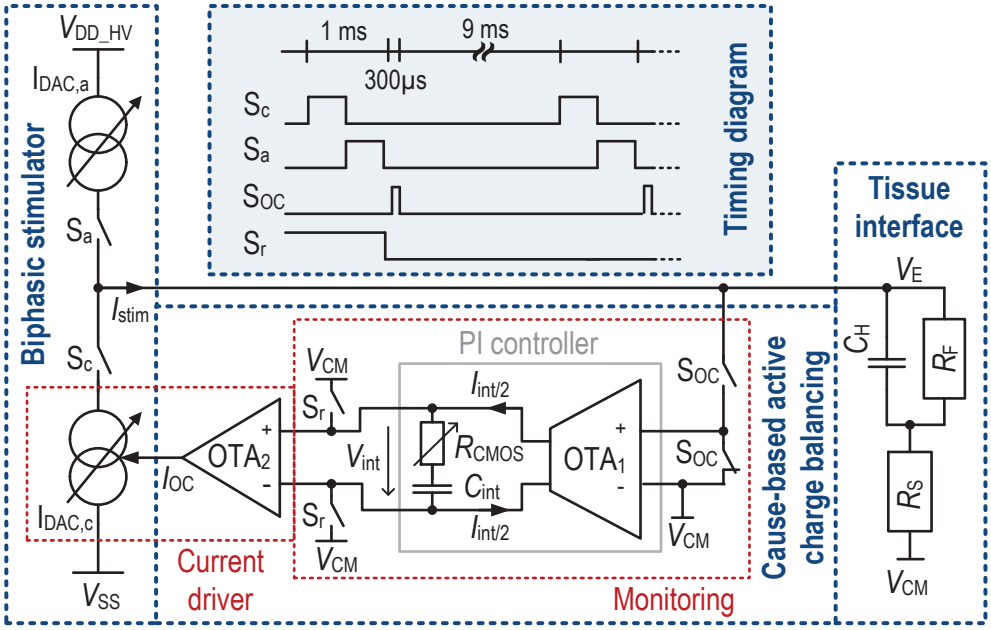


Figure 5.1.: System overview of the PI-controlled OC, consisting of the PI controller and interface OTA_2, including an exemplary timing diagram.

design, cathodic stimuli adjustment was chosen due to the following reasons: First, the OTA_1 architecture was built in a way that shifts the error signal into a LV domain to save power in all further signal processing components. Choosing the LV domain close to V_{SS} instead of V_{DD_HV} allows to use smaller devices, since no isolated transistor process is needed, and thus, the well constraints are reduced. Second, the settling process of the control loop might lead to some overshoots, resulting in an increased current amplitude. However, defining the anodic stimulus amplitude is a sensitive process which should not be manipulated, since too high anodic currents could trigger unwanted AP within the neuron.

The compensation concept is illustrated in Fig. 5.2. I_{OC} is regularly adjusted to match the biphasic stimuli, which keeps V_E at V_{CM} with respect to the loop accuracy range that is well below the safety limits. The overall concept resembles the offset regulation of [9]. However, the circuit implementation is fundamentally different since this work aims at a low-power integrated CMOS design instead of a PCB-implemented circuit. State-of-the-art charge balancing systems typically check the value of the remaining V_E against a safety window for a short time during the measurement period by a comparator. In this implementation, no window comparator is necessary. Further, the control behavior was analyzed and optimized in this work. Instead of an I or PT controller [9], a PI controller was chosen since it offers one additional degree of freedom to adapt to a wide variety of electrodes.

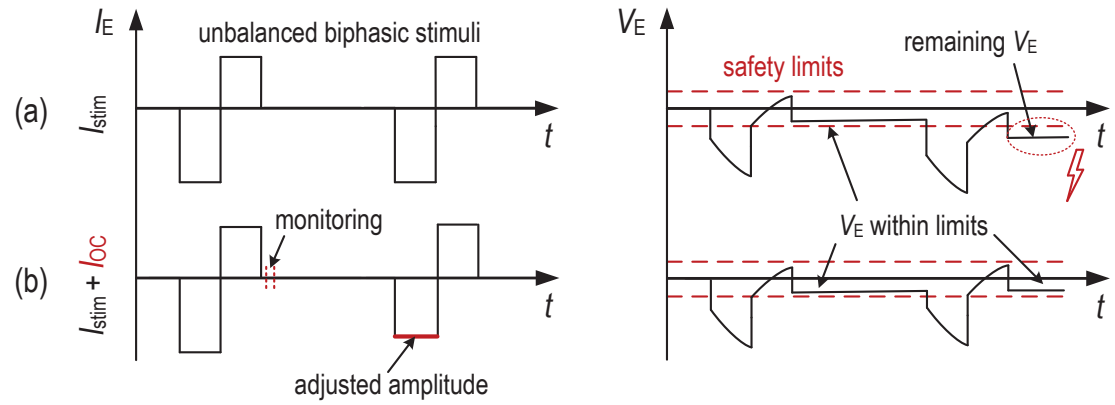


Figure 5.2.: Sketch of the compensation concept, depicting in (a) the rise of a remaining voltage V_E for unbalanced biphasic current pulses I_{Stim}. In (b) the stimuli is adjusted by the compensation current I_{OC}, keeping V_E within the safety limits.

5.2. Controller Considerations

The core of the proposed OC circuit is the CMOS integrated controller. A design challenge was the low-frequency signal processing application, i.e. storing the mismatch information for several stimulation periods. Via an integration, a memory like behavior is provided and the corresponding offset current can be spread over time [9]. However, this implies a very large time constant τ in the order of few milli-seconds, while avoiding large resistance values and keeping the capacitance reasonably small for a small die area. Therefore, in contrast to the operational amplifier approach that uses large RC values in a feedback configuration [9], the proposed integrated CMOS solution takes advantage of a transconductance-capacitance (G_m-C) based integrator approach in an open loop configuration. Thus, the passive resistor R is replaced by the $1/G_m$ value of the OTA_1 [73]. G_m-C techniques with very small transconductance allow the on-chip capacitance to be kept manageably low [74, 75]. Furthermore, superior performance in terms of power consumption and time constant is expected when compared to a feedback operational amplifier concept [73–75]. An ideal OTA has the transfer characteristic of a voltage controlled current source

$$I_{int} = G_m \cdot V_{in} \,, \tag{5.1}$$

where the output current I_{int} is directly proportional to the input voltage V_{in} by its overall G_m. Single ended as well as fully differential implementations are possible. The latter was chosen for symmetry reasons, and because the subsequent component OTA_2 provides a differential input.

The initial G_m-C integrator design [72] was further developed to a G_m-RC based PI controller [13, 63]. The latter provides an additional zero z_{PI} (Fig. 5.3(a)), and therefore, was seen as beneficial in terms of stability by means of pole-zero compensation,

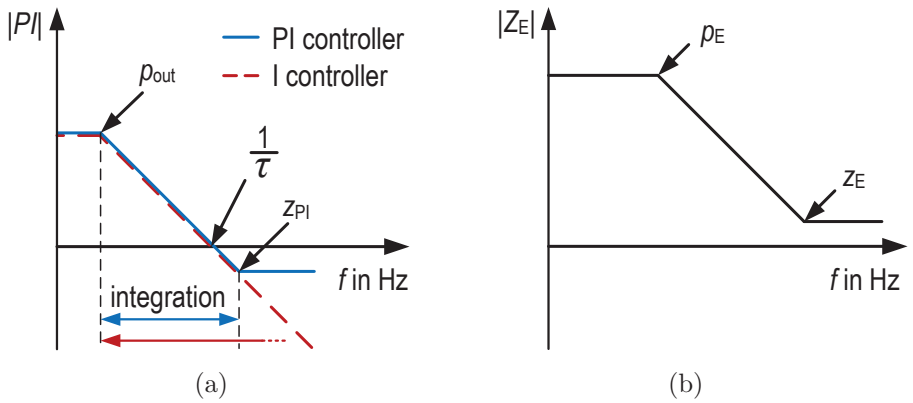


Figure 5.3.: Magnitude plot of (a) a non-ideal I and PI controller transfer function, and (b) electrode impedance $Z_{\mathrm{E}}(s)$ [13] (©2018, IEEE).

considering a dominant pole of the electrode impedance (Fig. 5.3(b))

$$p_{\mathrm{E}} = \frac{1}{C_{\mathrm{H}} R_{\mathrm{F}}}, \tag{5.2}$$

due to large R_{F} values. Whereas, the electrode zero

$$z_{\mathrm{E}} = \frac{1}{C_{\mathrm{H}}(R_{\mathrm{S}} \parallel R_{\mathrm{F}})} \tag{5.3}$$

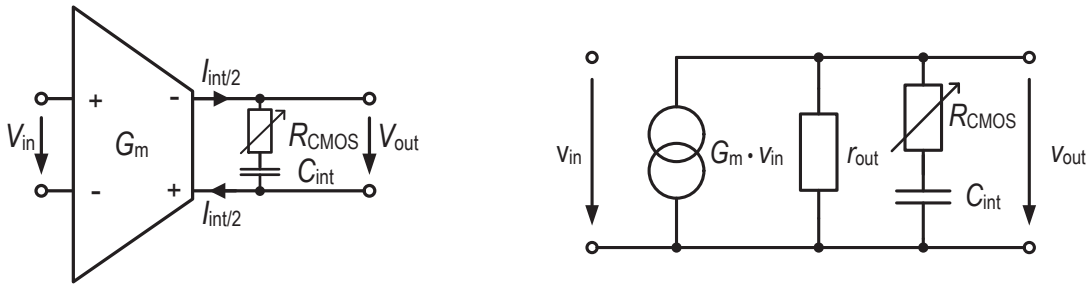
is mainly defined by C_{H} and R_{S}, since R_{S} is typically much smaller than R_{F}, and therefore, lies at higher frequencies. The value of p_{E} and z_{E} differ between electrodes, and thus, change the overall settling behavior, which demands for an adjustable control. Fig. 5.4 illustrates the fully differential OTA$_1$-$R_{\mathrm{CMOS}}C_{\mathrm{int}}$ controller, and its small signal equivalent model. The R_{CMOS} value of the PI controller is tunable. In case of a zero resistance value, the function is replaced by the proposed G_{m}-C integrator of [72]. The finite output resistance r_{out} of OTA$_1$ limits the DC gain. The transfer function of the non-ideal integrator $I(s)$ results in

$$I(s) = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = \frac{G_{\mathrm{m}} \cdot r_{\mathrm{out}}}{1 + s \cdot C_{\mathrm{int}} \cdot r_{\mathrm{out}}} \overset{r_{\mathrm{out}} \to \infty}{=} \frac{G_{\mathrm{m}}}{s \cdot C_{\mathrm{int}}}, \tag{5.4}$$

where s is the Laplace operator. The frequency response approaches ideal integration behavior with infinite DC gain by increasing r_{out} to infinity. Introducing R_{CMOS} to the non-ideal G_{m}-C integrator, yields to the PI controller transfer function:

$$PI(s) = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = \frac{G_{\mathrm{m}} \cdot r_{\mathrm{out}} \cdot (1 + s \cdot C_{\mathrm{int}} \cdot R_{\mathrm{CMOS}})}{1 + s \cdot C_{\mathrm{int}} \cdot (r_{\mathrm{out}} + R_{\mathrm{CMOS}})} \overset{r_{\mathrm{out}} \to \infty}{=} \frac{G_{\mathrm{m}} \cdot (1 + s \cdot C_{\mathrm{int}} \cdot R_{\mathrm{CMOS}})}{s \cdot C_{\mathrm{int}}}. \tag{5.5}$$

The non-ideal I controller, as formulated in Eq. (5.4), is compared to the here recommended non-ideal PI controller of Eq. (5.5) by illustrating their transfer characteristics in Fig. 5.3(a). As long as $R_{\mathrm{CMOS}} \ll r_{\mathrm{out}}$ holds, both controls provide a



(a) (b)

Figure 5.4.: (a) Block diagram of the G_m-RC components, and (b) showing its small signal equivalent circuit.

low-frequency pole defined by

$$p_\mathrm{out} \approx \frac{-1}{C_\mathrm{int} r_\mathrm{out}} \,. \tag{5.6}$$

The non-ideal I controller represents a one pole system, whereas the PI controller does provide the additional zero

$$z_\mathrm{PI} = \frac{-1}{C_\mathrm{int} R_\mathrm{CMOS}} \,. \tag{5.7}$$

At frequencies larger than p_out and smaller z_PI, the magnitude drops by 20 dB per decade, equivalent to an ideal integration behavior with time constant

$$\tau = \frac{C_\mathrm{int}}{G_\mathrm{m}} \,, \tag{5.8}$$

adjustable by the choice of C_int and G_m of OTA_1. However, in this charge balancing application, it was not necessary to precisely achieve a predefined nominal value of τ. Little deviations lead to minor changes in the speed of integration but are not crucial for a proper functionality, and could be compensated by adjusting the time of integration.

5.3. Components Design and Characterization

The PI-controlled OC consists of the OTA_1-$R_\mathrm{CMOS}C_\mathrm{int}$ controller and the OTA_2 current driver that interfaces the cathodic current DAC. Implementing the system as a low-power but HV-robust circuit is advicable. Beside the very low transconductance, inherent features like a HV to LV level shift and good output current linearity for a wide input voltage range are provided.

5.3.1. PI Controller

The detailed description of the controller design and characterization is structured and subdivided according to its four main features[6] that are: providing (a) a very small and linear transconductance at (b) a wide input voltage range with (c) an inherent voltage level shift, and (d) a high flexibility in terms of controller settings.

(a) 1.5 nS Transconductance: To meet the requirement of a time constant in the milli-second range with reasonable small on-chip integration capacitance C_{int}, a very small overal G_{m} of the controller in the nano-siemens range is required. Several possible approaches had been considered, including current division, current cancellation, implementation of triode region input pairs and cascading of transconductance-transimpedance stages [73–78]. Based on comparative simulations and the results of [73, 77, 78], a very small transconductance and a wide linear input range were obtained best by current cancellation via cross-coupled differential pairs, operating in saturation. The PI controller design is shown in Fig. 5.5. Two differential input pairs $\mathrm{M}_{1,2}$ with different transistor sizes and tail currents are connected anti-parallel to each other. The respective g_{m} of the input pairs are subtracted from each other,

$$G_{\mathrm{m}} = g_{\mathrm{m1}} - g_{\mathrm{m2}}\,, \tag{5.9}$$

which can lead to a very small overall G_{m}, here designed to be around 1.5 nS.

Additionally, using cross-coupled differential input pairs allows for an improved linearity by adjusting the tail currents I_{SS} and transistor dimensions in a way, that the 3^{rd} order distortion of the output current I_{int}, which corresponds to the 2^{nd} order distortion of the overall G_{m}, cancels [78]. To examine the linearity, the small signal g_{m} of a single differential source-coupled pair is derived and shown for transistor pair M_1. All transistors operate in saturation. Following the steps of [79] chapter 10.3.2 and applying a differential input voltage V_{di} results in the large signal currents for the two M_1 transistors

$$I_{\mathrm{D1}} = \frac{I_{\mathrm{SS1}}}{2} + \frac{V_{\mathrm{di}}}{4} \cdot \sqrt{\beta_1 \cdot [4I_{\mathrm{SS1}} - \beta_1 \cdot V_{\mathrm{di}}^2]} \tag{5.10}$$

and

$$I'_{\mathrm{D1}} = \frac{I_{\mathrm{SS1}}}{2} - \frac{V_{\mathrm{di}}}{4} \cdot \sqrt{\beta_1 \cdot [4I_{\mathrm{SS1}} - \beta_1 \cdot V_{\mathrm{di}}^2]}\,. \tag{5.11}$$

The resultant differential current of the transistor pair M_1 is

$$I_{\mathrm{D1}} - I'_{\mathrm{D1}} = \frac{1}{2} \cdot \beta_1 \cdot V_{\mathrm{di}} \cdot \sqrt{\frac{4I_{\mathrm{SS1}}}{\beta_1} - V_{\mathrm{di}}^2}\,. \tag{5.12}$$

[6] Concerning feature (a) - (c), design considerations on a transistor level have been performed within the preliminary work [15] of the author of this thesis.

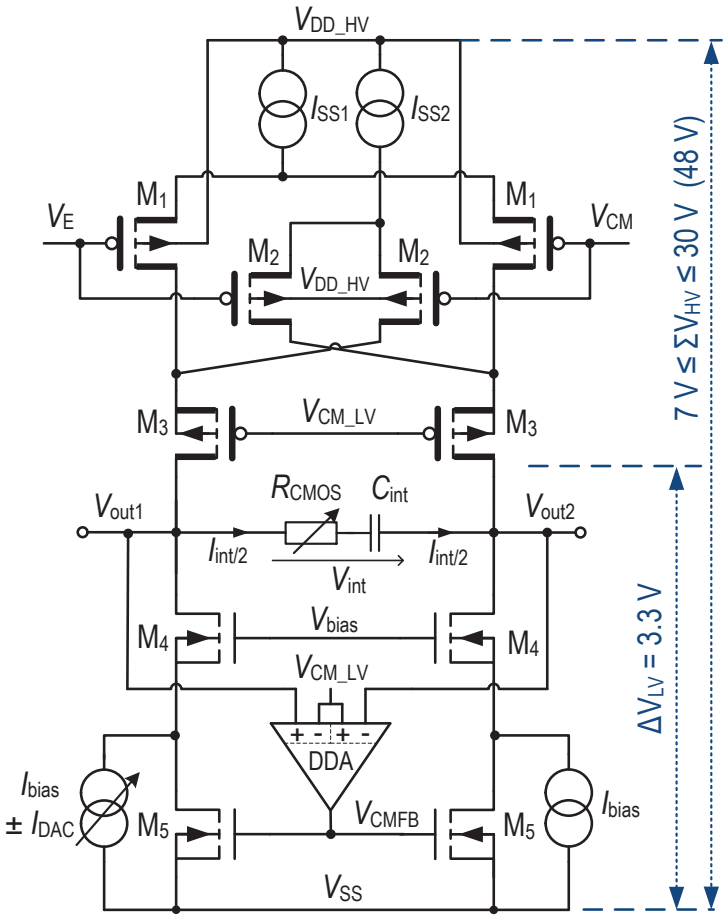


Figure 5.5.: Transistor-level implementation of the PI controller (OTA_1). Mordified from [72] (©2014, IEEE).

Its derivative with respect to V_{di} yields to

$$g_{\mathrm{m1}} = \frac{dI_{\mathrm{D1}} - dI_{\mathrm{D1}}}{dV_{\mathrm{di}}} = \frac{2I_{\mathrm{SS1}} - \beta_1 \cdot V_{\mathrm{di}}^2}{\sqrt{\frac{4I_{\mathrm{SS1}}}{\beta_1} - V_{\mathrm{di}}^2}}\,. \tag{5.13}$$

Applying the Taylor series expansion at the point V_{di}=0 V, g_{m} is expressed by

$$g_{\mathrm{m1}} = \sqrt{\beta_1 \cdot I_{\mathrm{SS1}}} - \frac{3}{8} \cdot \sqrt{\frac{\beta_1^3}{I_{\mathrm{SS1}}}} \cdot V_{\mathrm{di}}^2 - \frac{5}{128} \cdot \sqrt{\frac{\beta_1^5}{I_{\mathrm{SS1}}^3}} \cdot V_{\mathrm{di}}^4 - \ldots\,. \tag{5.14}$$

The first order term is independent of V_{di}. It thus becomes obvious, that nonlinearities arise from higher order terms. Decreasing β suppresses the influence of these terms and a better linearity can be achieved. Therefore, a ratio of (W/L)<1 was chosen in this design. Further, the four input transistors $M_{1,2}$ were arranged as two crossed-coupled differential pairs (Fig. 5.5), increasing the linearity by eliminating the 3rd order distortion of I_{int} [78]. Extracted from the Taylor approximation

Eq. (5.14), the gain requirement yields

$$G_{\mathrm{m,2rd}} = g_{\mathrm{m1,2rd}} - g_{\mathrm{m2,2rd}} = \frac{3}{8} \cdot \left(\sqrt{\frac{\beta_1^3}{I_{\mathrm{SS1}}}} - \sqrt{\frac{\beta_2^3}{I_{\mathrm{SS2}}}} \right) \cdot V_{\mathrm{di}}^2 \stackrel{!}{=} 0\,, \tag{5.15}$$

which can be expressed as

$$\frac{I_{\mathrm{SS1}}}{I_{\mathrm{SS2}}} \stackrel{!}{=} \left(\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \right)^3 . \tag{5.16}$$

To realize the very small tranconductans of around 1.5 nS, the ratio in Eq. (5.16) must be close to one. It was set to around 1.04 by I_{SS1} of 250 nA and I_{SS2} of 240 nA. The requirement was best met by W/L dimensions of 5 µm/928 µm for M_1 and 4.9 µm/928 µm for M_2. [72] (©2014, IEEE). Monte Carlo simulation results of G_{m} and the resultant τ are listed in Tab. 5.1.

Table 5.1.: Results of a Gaussian distributed Monte Carlo simulation with 200 runs at 37°C and a 30 V supply.

	unit	typical	mean	σ
G_{m}	nS	1.59	1.60	0.08
τ	ms	7.54	7.55	0.39

(b) 6 V Input Range: An analog response instead of quantized integration steps of the output voltage V_{int} of the controller is guaranteed as long as the differential input voltage (V_{E}-V_{CM}) stays within the dynamic input range of OTA_1. The dynamic input range was defined by considering worst case conditions of 30% current mismatch at a stimulation current amplitude of ±10 mA applied for 1 ms, and an electrode setup with C_{H} of 1 µF. Thus, the input voltage rises up to

$$V_{\mathrm{E}} - V_{\mathrm{CM}} = \frac{30\% \cdot I_{\mathrm{stim}} \cdot t_{\mathrm{w}}}{C_{\mathrm{H}}} = \pm 3\,\mathrm{V}\,. \tag{5.17}$$

However, covering such a wide input range comes at the cost of die area, since it demands for a small W/L ratio of the input transistors ($M_{1,2}$) in the inherently larger HV-transistor type. Compared to LV transistors the minimum possible width is increased by a factor of around 12, resulting in an active area multiplied by 144. The achieved input range of ±3 V led to $(\mathrm{W/L})_{1,2}$ of 5 µm/928 µm. Especially long input transistors will be affected by linear gradients of process variations within a chip, which might increase the offset voltage of the OTA_1. Therefore, each of these very long input transistors was divided into 16 unit transistors of L of 58 µm each, connected in series. Special care was taken during layout for proper transistor

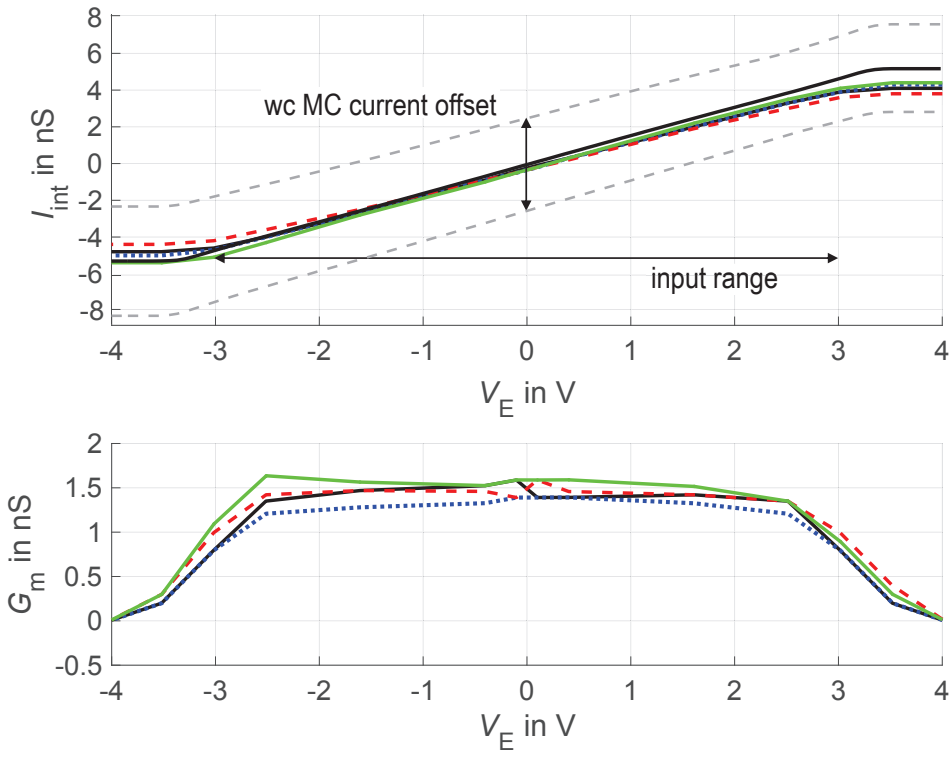


Figure 5.6.: OTA_1 characteristics of the output current I_{int}, including the worst case results of a Gaussian distributed Monte Carlo simulation, and overall transconductance G_m measured for four chips at ΣV_{HV} of 30 V [13] (©2018, IEEE).

matching. The layout was based on a two dimensional common centroid structure, which compensates linear gradients. The area requires 150 µm × 600 µm which is around 50% of the die area of the OTA_1 (see Fig. 5.13). However, for LV stimulators, or if smaller stimulus amplitudes, pulse widths, or mismatch are expected, the analog integration is still preserved at a smaller input range requirement of OTA_1, which will significantly reduce the active area. Further area reduction that may lead to an operation outside the dynamic input range, is also possible without hindering the functionality of the system. However, this would result in quantized integration steps until V_E is decreased within the dynamic input range.

Due to the expected worst case Monte Carlo deviations of I_{int}, illustrated in Fig. 5.6, an offset adjustment by a 6 bit current DAC with one additional bit assigned for offset direction was included in the OTA_1 design (see I_{DAC} in Fig. 5.5). However, the measured offset scatter was much less than expected from simulation, which is achieved by a good matching of the common centroid layout. Additionally, the measured offset was mainly in one and the same direction. The reason lies in the effect of the HV PMOS wells of the input stage that form a pn-junction with sensitivity to light. The evolved parasitic photo diode of the input stage is large enough to influence the output current I_{int}, which is then measured in form of an offset voltage V_{int}. However, this effect was easily reduced by a dark measurement setup, and will

be insignificant after chip housing. Within the four measured chips under a dark measurement setup, a maximum of two bits were sufficient for offset correction. The main OTA_1 characteristics I_{int} and overall G_{m}, measured for four chips after offset correction, are presented in Fig. 5.6. Within a wide linear input range of up to $\pm 3\,\mathrm{V}$ the overall G_{m} is 1.5 nS only. In this way, a reasonable small C_{int} of 12 pF is sufficient to achieve a time constant τ of 8 ms.

(c) HV to LV Level Shift: A voltage shift from input to output allows combining HV stimulation with LV signal processing, reducing the power consumption of subsequent components. The output level of the implemented OTA_1 is shifted from an overall HV environment $\Sigma \mathrm{V}_{\mathrm{HV}}$, which can lie between 7 V to 30 V, into the ΔLV domain of 3.3 V. In this implementation, where the bulk terminals of the input transistors are connected to $V_{\mathrm{DD\_HV}}$ due to layout reasons, the maximum voltage compliance is restricted by the the gate-bulk voltage V_{GB} of minimal $-30\,\mathrm{V}$ in the employed HV technology. This minimally allowed voltage will be reached in the case that the input voltage equals V_{SS}. However, connecting the bulk to the source terminal instead would increase the voltage compliance to 48 V. Here, the limiting condition is the gate-drain voltage V_{GD} of the input transistors in an extreme case, where V_{G} equals $V_{\mathrm{DD\_HV}}$. If a lower HV environment of the stimulator setup is sufficient for the application, the supply voltage of the OTA_1 can be reduced to a minimum of 7 V without any significant change of its characteristics. This lower limit results from the minimum voltage V_{GS} of the input transistors to work in saturation, which is around 3.2 V, in addition to the minimum required voltage drop of the upper current mirror of around 0.3 V. Reducing the supply voltage further is possible, however, this will decrease $I_{\mathrm{SS1,2}}$, and thus, change the working condition. At $\sum \mathrm{V}_{\mathrm{HV}}$ of 6 V, G_{m} is reduced to 1.3 nS and would becomes as low as 300 pS at $\sum \mathrm{V}_{\mathrm{HV}}$ of 3.3 V.

The HV to LV voltage level shift is carried out by a common mode feedback (CMFB) differential difference amplifier (DDA), included in Fig. 5.5. The LV output CM voltage $V_{\mathrm{CM\_LV}}$ is controlled to 1.65 V. The DDA output voltage

$$V_{\mathrm{CMFB}} = A \cdot \left(\frac{(V_{\mathrm{out1}} + V_{\mathrm{out2}})}{2} - V_{\mathrm{CM\_LV}} \right) \tag{5.18}$$

drives one part of the bottom current source (M_5), whereas the other part consists of a current source with a constant bias current I_{bias} plus a 7 bit current DAC (I_{DAC}) for offset adjustments. The I_{DAC} adjustment can be performed in a calibration step with a LSB of 125 pA. The cascoded transistors M_3 and M_4 of the OTA_1 were included to increase its output resistance r_{out}, which is wanted for an almost ideal integration, see Eq. (5.4) and Eq. (5.5). The output voltage V_{out} equals the drain voltages V_{D} of $\mathrm{M}_{3,4}$. M_3 is exposed to $\Sigma \mathrm{V}_{\mathrm{HV}}$, and therefore, is of a HV PMOS type. Further, M_3 is biased in a way to protect the output and $\mathrm{M}_{4,5}$ from HV

$$V_{\mathrm{out,max}} = V_{\mathrm{D3,4}} \leq V_{\mathrm{G3}} - V_{\mathrm{th3}}\,. \tag{5.19}$$

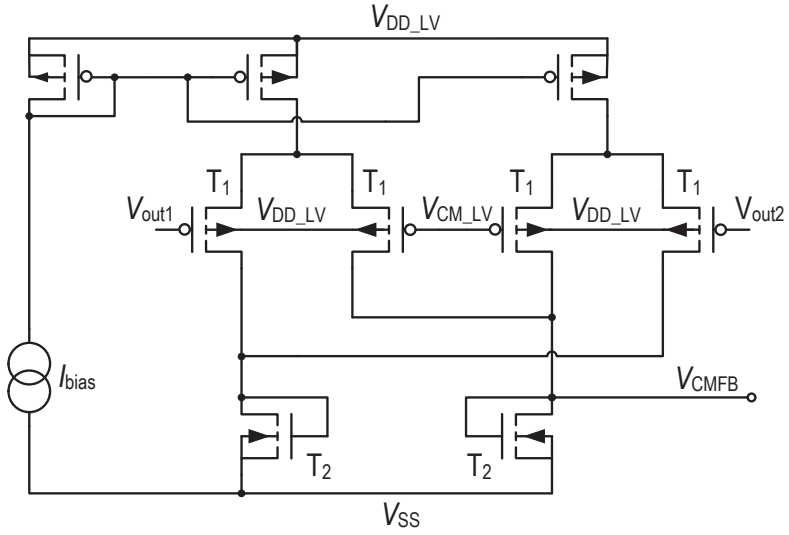


Figure 5.7.: DDA architecture for CMFB generation.

With the bulk connected to the source, M_3 exhibits a threshold voltage V_{th3} of around -1 V. Applying a bias voltage to V_{G3} of 1.65 V, which corresponds to V_{CM_LV}, M_3 restricts the output voltage in saturation to a maximum of 2.65 V. Protected by M_3, transistor M_4 is of an isolated LV NMOS type. Its bulk terminal is also connected to its source, providing a constant threshold voltage V_{th4} of 500 mV. The bias voltage V_{bias} is 1.15 V, limiting the minimum output voltage in saturation to 650 mV. Thus, a total output range of ±1 V symmetrical to $V_{CM,out}$ was achieved.

A standard CMFB DDA architecture, shown in Fig. 5.7, was chosen and designed with large input transistors T_1 to cover the output range of OTA_1. Each transistor T_1 is composed out of four unit elements with (W/L) = 600 nm/15 µm connected in series for a good common centroid layout matching. The overall CMFB loop gain was expected to be very large due to the high cascade-load of the OTA_1 in addition to the open loop gain of the DDA, which might be critical for a stable operation. Therefore, to reduce the CMFB loop gain, diode-connected loads T_2 were chosen. The CMFB loop stability was proven by simulations, providing a phase margin of greater than 60 °. One distinct dominant pole at 8 mHz is defined by the large integration capacitance C_{int} and the output resistance of OTA_1. The second pole at 375 kHz arises at the DDA output due to the small resistance of the diode-connected transistor T_2 (Fig. 5.7) and a small parasitic capacitances of M_5 of the OTA_1 (Fig. 5.5).

(d) 5 Bit R_{CMOS} Setting A further controller requirement is to provide an adjustable settling behavior in order to adapt to different electrode parameters and their long-term impedance degradation. This can be reached by on-chip trimming of the resistor R_{CMOS}. Therefore, R_{CMOS} was realized by a switchable array of eight unit resistances R_{1-8}, arranged as shown in Fig. 5.8. Each resistance consists of a

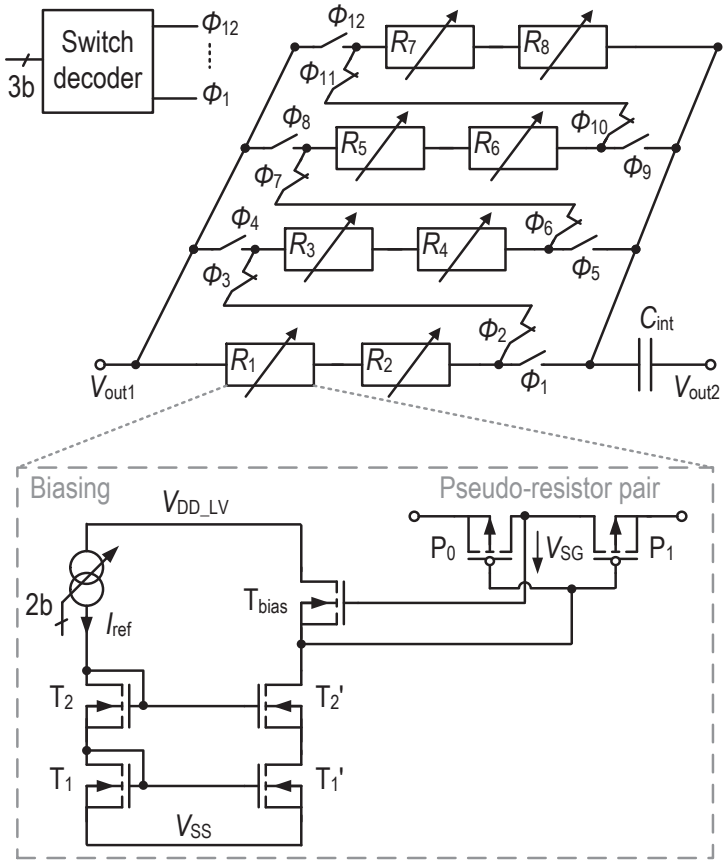


Figure 5.8.: Schematic of the R_{CMOS} implementation. Modified from [13] (©2018, IEEE).

pseudo-resistor PMOS pair based on [80], which can provide resistances in the giga-ohm range at a small die area. For symmetry reasons, the source terminals of each PMOS pair P_0 and P_1 were connected back-to-back. The bulk of each transistor was connected to its drain terminal. The transistors operate in subthreshold region, providing a very high linear resistance across their drain-source terminals. Derived from [80], the resistance for one transistor can be formulated as

$$R_{\mathrm{SD}} = \frac{1}{G_{\mathrm{SD}}} = \frac{L}{2n\beta_0 W V_{\mathrm{T}} G_{\mathrm{SD0}}} \cdot e^{\frac{|V_{\mathrm{th}}| - V_{\mathrm{SG}}}{nV_{\mathrm{T}}}}, \tag{5.20}$$

where G_{SD0} is the output conductance at zero source-drain voltage, V_{T} is the thermal voltage (typically around 25 mV) and n is the subthreshold slope factor of the PMOS device (typically in the range of 1-2). With the gates of P_0 and P_1 connected, their total resistance is configurable by the applied source-gate voltage V_{SG}. V_{SG} is defined by a biasing circuit and depends on the dimensions of the implemented common drain transistor $\mathrm{T}_{\mathrm{bias}}$ as well as the applied biasing current that can be set to 5 nA, 15 nA or 40 nA. In total, R_{CMOS} is adjustable from 0 Ω to 12 GΩ by 5 bits.

5.3.2. Current Driver

The voltage to current conversion of the integrated and stored voltage V_{int} was achieved by a single ended LV architecture of OTA_2, as shown in Fig. 5.9. Its transconductance was linearized for an input voltage range of ±500 mV by resistive source degeneration [81]. The drain terminals of the input transistors M_1 are connected via a degeneration resistor R_{deg}. This reduces the voltage swing of $V_{\mathrm{GS},1}$, and thus, increases the transconductance linearity. In saturation, the overall G_{m} results to

$$G_{\mathrm{m}} = \frac{g_{\mathrm{m1}}}{(1 + g_{\mathrm{m1}} \cdot R_{\mathrm{deg}})}\,, \tag{5.21}$$

where g_{m1} is defined by the bias current I_{SS} and transistor dimensions. In order to achieve a wide linear input range, large resistors are needed, leading to an overall G_{m} expressed by

$$G_{\mathrm{m}} \overset{g_{\mathrm{m1}} \to 1}{\approx} \frac{1}{R_{\mathrm{deg}}}\,. \tag{5.22}$$

Instead of implementing a large resistor, R_{deg} was replaced by two MOS transistors operating in triode region, consuming smaller silicon area.

The resultant output current I_{OC} is directly added to the biasing current of the cathodic stimulation $\mathrm{I}_{\mathrm{DAC,c}}$, thus correcting the intensities of positive and negative stimulation percentage wise. Small currents I_{OC} with a maximum of ±40 nA are already sufficient to compensate around ±36% of charge mismatch in $\mathrm{I}_{\mathrm{DAC,c}}$, independent of the absolute output current that might become as high as ±10 mA.

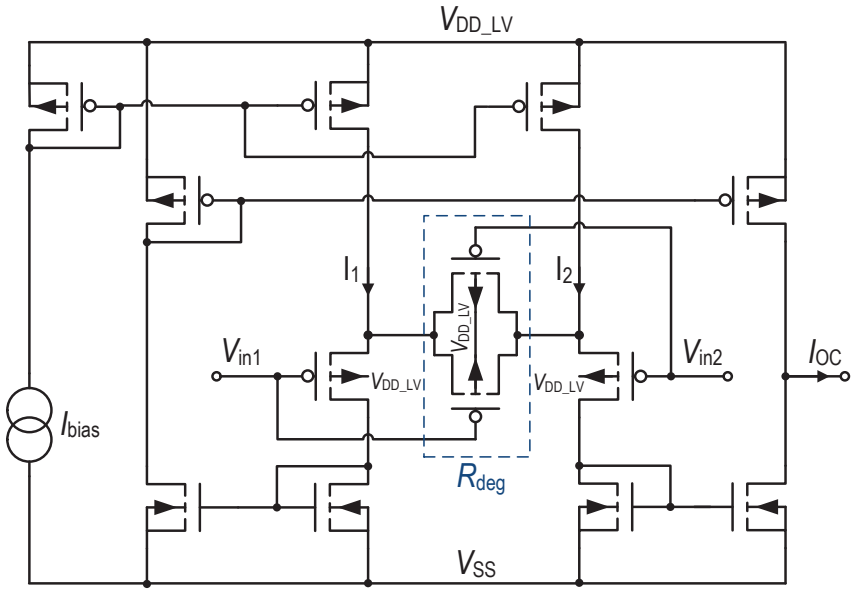


Figure 5.9.: Schematic of the proposed interface OTA_2, including source degeneration using MOS transistors.

5.4. Stability Considerations

Offset compensation methods represent closed loop systems, whose stability is dependent on the system condition and the electrode setup. The presented PI-controlled OC circuit is converted into the standard control representation, shown in Fig. 5.10. The controller of the loop is $PI(s)$ with output voltage V_{int}, followed by a transconductance gain stage (considered as ideal), consisting of the G_{m} of OTA_2 and an additional gain $A_{\mathrm{I_{DAC,c}}}$, which is dependent on the setting of the cathodic $\mathrm{I_{DAC,c}}$. The system is defined by the impedance $Z_{\mathrm{E}}(s)$ of the electrode-tissue interface. Via a direct feedback path, V_{E} is subtracted from the target value, which is the body's quiescent potential V_{CM}. Typically, the electrode provides a pole at very low frequencies, and thus, its transfer characteristic $Z_{\mathrm{E}}(s)$ is interacting with the transfer characteristic $PI(s)$ of the controller. Therefore, special care must be taken by choosing an appropriate controller. As an advantage of the implemented configurable PI controller over an I controller, an adequate positioning of the additional zero z_{PI} allows for stability adjustments by means of pole-zero compensation, which is tested and proven by simulation and chip measurements.

The adjustability of the control to a given electrode with electrical equivalent parameters of C_{H} of 0.1 µF, R_{F} of 10 MΩ, and R_{S} of 1 kΩ was analyzed by its open loop characteristic, which is shaped by $PI(s)$ multiplied with $Z_{\mathrm{E}}(s)$. In Fig. 5.11(a) the results are presented in form of a simulated bode plot, and in (b) the corresponding simulated and measured transient responses at the controller output V_{int} are given. The red curve shows the case for an I control, for which in the presented design (Fig. 5.5) R_{CMOS} was shorted. Typically, both poles p_{out} and p_{E} lie at very low frequencies due to their large RC-values. If an I control only is used, the distance between the second pole and z_{E} becomes crucial for stability. In this example, p_{out} and p_{E} are very close to each other. The zero z_{E} however, lies at much higher frequencies, since $R_{\mathrm{F}} \gg R_{\mathrm{S}}$. Thus, the phase margin (PM) results to 3° only, which causes large overshoots and long transient settling times. Therefore, it is an advantage of the presented system to use a PI controller instead of an I controller, by introducing and adjusting the value of R_{CMOS}. The additional zero z_{PI} can be placed before z_{E}, i.e. close to the second pole so that the phase rises,

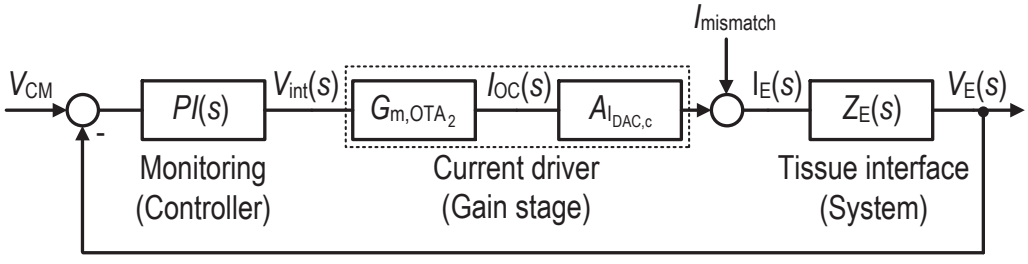


Figure 5.10.: The PI-controlled OC circuit in its standard loop representation. Adjusted from [13] (©2018, IEEE).

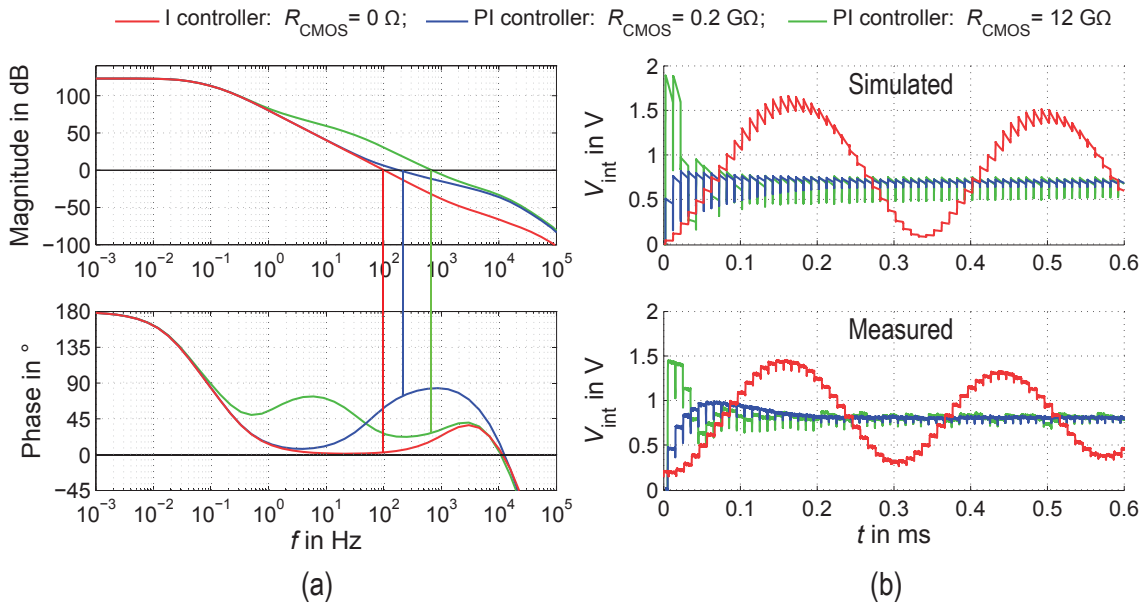


Figure 5.11.: (a) Simulated bode plot of the PI-controlled OC in its open loop configuration for three different R_{CMOS} settings, and (b) the corresponding simulated transient response of the closed loop system, which is compared with the measurement results for an electrode equivalent model with C_{H} of 0.1 µF, R_{F} of 10 MΩ, and R_{S} of 1 kΩ [13] (©2018, IEEE).

and thereby, the PM increases. Dependent on the electrode parameters, it might be even possible to do complete pole-zero compensation by shifting z_{PI} onto p_{E}. Thus, a stable one pole system with 90° phase margin will be developed. Additional poles due to parasitic capacitances within the circuit are visible in the bode plot but not crucial, since they occur at frequencies above 10 kHz. A fast and smooth settling was found by a PI control with R_{CMOS} of 200 MΩ that results in a PM of 71°, see Fig. 5.11 (blue line). Further increasing R_{CMOS} to 12 GΩ (green line), places z_{PI} in closer proximity to the second pole. However, not only the phase, but also the unity gain frequency rises, which results in a PM of 60° providing a fast settling with one distinct overshoot.

Fig. 5.11 demonstrates the adjustability of the PI control to any given electrode. However, this does not yet give information about the control behavior for a changing load. Therefore, based on a good system setting with R_{CMOS} of 0.2 GΩ as found in Fig. 5.11, three simulations scenario are demonstrated in Fig. 5.12. In each simulation one electrode parameter changes significantly, while the others stay constant. A change in R_{S} influences the location of z_{E}. However, varying R_{S} from 0.1 kΩ to 5 kΩ shows no influence on the transient behavior (Fig. 5.12(b)). In Fig. 5.12(c) R_{F} was changed by a factor of 200, from 0.5 MΩ to 100 MΩ. Even though the location of p_{E} was effected this time, none significant influence on the settling is visible. Varying C_{H} (Fig. 5.12(a)), and thus, the location of p_{E} and z_{E}, will change

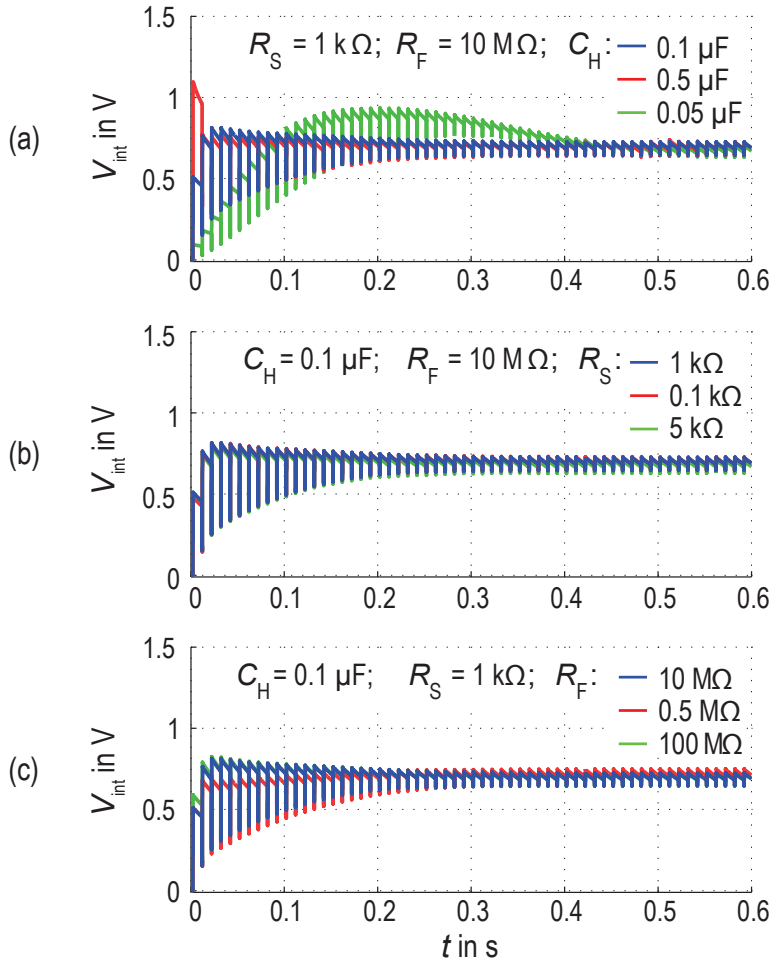


Figure 5.12.: Simulated behavior for the PI-controlled OC for changing electrode parameters. In (a) C_H, in (b) R_S, and in (c) R_F was changed. The controller setting was chosen with R_{CMOS} of 0.2 MΩ, based on the results of Fig. 5.11 [13] (©2018, IEEE).

the transient response most. However, a change in the range of a factor of 10 from 0.05 µF to 0.5 µF still shows a sufficiently good settling. Thus, the simulation results of Fig. 5.12 prove that once a stable setting for a given electrode is chosen, changes in the electrode parameters, for example due to tissue growth, will not significantly influence the settling behavior of the system and a recalibration is not needed.

5.5. Measurement Results

The components characterization and system measurements were mainly carried out by the chip, shown in Fig. 5.13. Additional monitoring buffers (Fig. 5.13 no. 8) were connected to the output of OTA_1 for better access during characterization. Further, the PI-controlled OC interfaces with an on-chip biphasic stimulator, which is one channel of the stimulator front-end described in sec. 4.3. The active area of the PI-controlled OC, comprising numbers 1 to 6, is less than 0.5 mm^2. Throughout the design, special care was taken to keep power losses at a minimum. Thus, even at a ΣV_{HV} environment of 22 V, the resultant measured power consumption of the PI-controlled OC was 18.9 µW only. By specifying the current consumption of each component in Tab. 5.2, the power losses can also be estimated for other supply voltages ΣV_{HV} between 7 V to 30 V.

5.5.1. System Measurements

The integrated biphasic stimulator and all switches $S_{a,c,OC,r}$ were programmed and controlled by an external field programmable gate array (FPGA), see sec. A.2. The stimulation frequency was 100 Hz, the pulse width $t_{wa,wc}$ was 500 µs each, and current

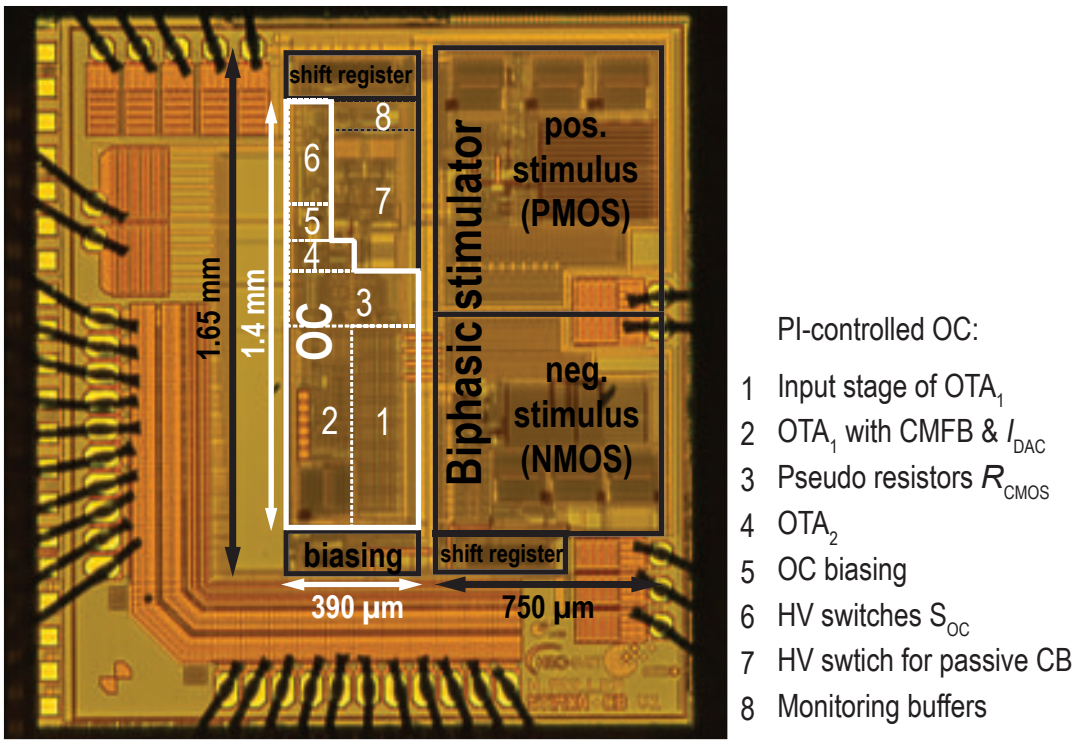


Figure 5.13.: Micrograph of the PI-controlled OC circuit integrated on a chip with the one channel biphasic stimulator. Modified from [13] (©2018, IEEE).

Table 5.2.: Power consumption of the PI-controlled OC in its monitoring steady state, listed by components.

Main components		OTA_1	CMFB DDA	R_{CMOS}	OTA_2	$2 \cdot S_{OC}$
Supply voltage	V	7 to 30	3.3	3.3	3.3	7 to 30
Current consumption	nA	610	220	80 to 640	240	40
Simulated total power	µW	8.2 to 23.2				
Measured total power	µW	18.9 at 22 V				

amplitudes were 1 mA with an intentional mismatch in cathodic stimulus of 20%. At the beginning of the measurement S_r was closed to reset V_{int}. Afterwards, S_{OC} was 'on' for 300 µs directly after each stimulus. The system was measured with an electrode equivalent model with C_H of 0.1 µF, R_F of 1 MΩ, and R_S of 1 kΩ, shown in Fig. 5.14. Without CB (black line) V_E increases with every stimulation pulse until it reaches a static state, at which the electrode self-discharge equals the stimulus mismatch charge. Thus, the electrode-tissue interface would be permanently exposed to a harmful DC potential of around 10 V. Using OC, it was possible to control the remaining V_E by adjusting the cathodic stimulus amplitude. The controller of the OC was changed from an I to a PI controller by changing the value of R_{CMOS}. In the second zoom, compared with the first zoom of I_E in Fig. 5.14, shows that the current mismatch was eliminated for both controllers. Once V_E settled, a remaining V_E of around ±20 mV was measured, which is significantly smaller than the safety window of ±50 mV or ±100 mV. However, the I control showed higher overshoots compared to the PI control. Thus, the PI controller allows to adjust the settling behavior by choosing an appropriate value of R_{CMOS} according to the system setup and conditions.

5.5.2. In-Vitro Measurements

The system was tested in an in-vitro environment with platinum electrodes of different sizes, as shwon in Fig. 4.13, in phosphate-buffered 0.9% saline solution. In-vitro measurement results via one of the smaller electrodes no. 20 are presented in Fig. 5.15. A stimulation pulse of 1 mA amplitude with 30% cathodic mismatch was intended. Without charge balancing the introduced mismatch would lead to a harmful permanent electrode potential. Using the PI-controlled OC, V_E was successfully kept within the safety window with an accuracy of −20 mV with respect to V_{CM}. It is visible in Fig. 5.15 that after a manual calibration of R_{CMOS}, the control exhibits a slight overshoot, however, manages to compensate the origin of the mismatch by adjusting the cathodic stimulus amplitude.

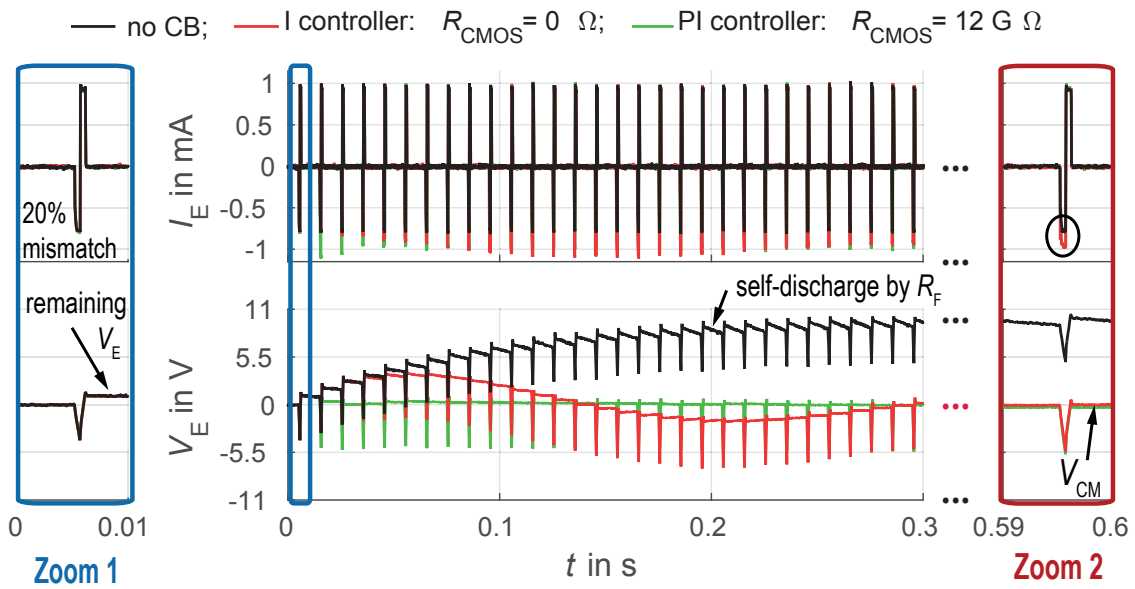


Figure 5.14.: System results of the PI-controlled OC, using an electrode equivalent model with C_H of 0.1 µF, R_F of 1 MΩ, and R_S of 1 kΩ. The results of a well-adjusted PI control (green) are compared to a non-balanced condition (black) and an I-controlled OC (red) [13] (©2018, IEEE).

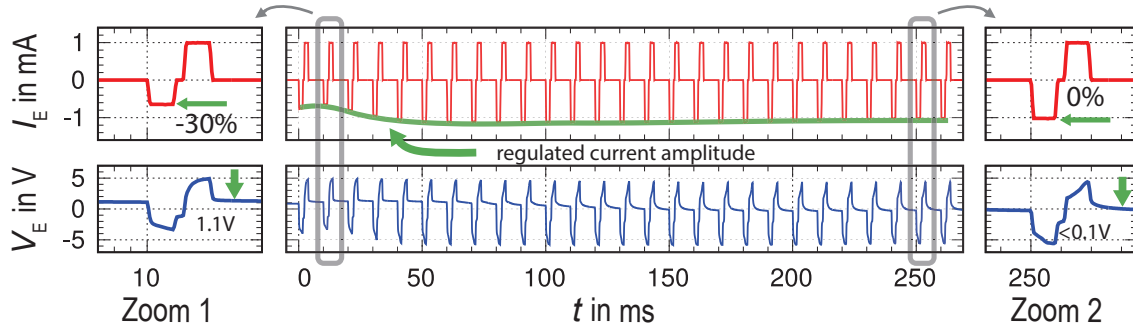


Figure 5.15.: In-vitro measurement results with a platinum electrode in 0.9% saline solution. A biphasic stimulation current I_E of 1 mA and 30% mismatch in the cathodic stimulus and its corresponding V_E during charge compensation via PI-controlled OC is shown. The starting condition and the settled condition are illustrated in the zoomed views. Modified from [61] (©2018, IEEE).

5.6. Comparison to State-of-the-Art Cause-Based Systems

The comparison in Tab. 5.3 benchmarks the performance of the presented PI-controlled OC against other state-of-the-art cause-based systems. This balancer not only provides a variable voltage compliance, but also the highest maximum voltage of 30 V compared with other integrated CB circuits. The comparison of power dissipation is difficult since most references lack a detailed power consumption description of the charge balancing circuit explicitly. The power consumption of the digital OC implementation of [4] is noted as 0.4 µW, reached by a duty cycle with very short activation time of the HV comparator within one stimulation interval. The actual time for the activation of the HV comparator is not given. However, the low-power design effort of the presented balancer becomes obvious when comparing it to the HV comparator design used in [4], which refers to [34] that documents the power dissipation of the HV comparator itself, which is more than 10-times larger. The presented analog implementation of this work has area disadvantages, especially when compared to the integrated digital OC solution of [4]. In contrast to [28, 31], where solely I_{Stim} is controlled, disregarding any kind of electrode-electrolyte voltage variations and errors, the publications [4, 9] as well as this work monitor and control V_{E}. The implemented OTA_1 design of this work is notable, since it provides an overall G_{m} of 1.5 nS only, and thus, achieves the large time constant of 8 ms with an on-chip capacitance of 12 pF. Therefore, in contrast to [9], this work offers miniaturization since it enables an on-chip implementation of an analog PI-controlled OC. The PI control system behavior is advantageous in terms of stability by means of pole-zero compensation, when compared to an I or PT control, since it offers one more degree of freedom to adapt to a wide variety of electrodes. The precision and compensation range of the digital OC is limited according to the number of bits. The PI-controlled OC is capable of up to ±36% biphasic stimuli mismatch correction with a measured compensation precision of ±20 mV with respect to the body's quiescent potential.

Table 5.3.: Comparison of state-of-the-art cause-based active charge balancers.

Reference	ISSCC 2012 [31]	JSSC 2015 [28]	TBioCAS 2010 [9]	JSSC 2012 [4]	**This work**
Cause-based CB method	Current matching	Charge monitoring	Analog OC	Digital OC	Analog OC
Process	0.13 µm	0.35 µm	Discrete (PCB)	0.35 µm	0.35 µm
Max. voltage compliance	3.3 V	4.2 V	30 V	20 V	30 V
Power consumption	N/A	N/A	N/A	0.4 µW** (438 µW ***)	23.2 µW
Die area	0.16 mm^2 *	0.33 mm^2 *	N/A	0.03 mm^2 ***	0.45 mm^2
Controlled variable	I_{Stim}	I_{Stim}	V_E	V_E	V_E
Controller	large time constant (>10 s) S/H circuit	Zero crossing detection	Tunable I or PT controller ($\tau = 4.7$ ms)	3-bit Moore state machine	Tunable I or PI controller ($\tau = 8$ ms)
Precision	Stimulus mismatch <10 nA	Charge mismatch <22 nC	remaining $V_E < \pm 100$ mV	remaining $V_E < \pm 100$ mV	remaining $V_E \lesssim \pm 20$ mV
Compensation range	N/A	N/A	N/A	±15% of biphasic current	±36% of biphasic current

*estimated

**assumed to be per duty cycle

***estimated from [34], because [4] refers to the HV comparator of [34]

5.7. Summary

Active CB was implemented in form of a PI-controlled Offset Compensation, which reaches a long-term charge balanced state at the tissue interface. Therefore, the residual electrode voltage of several subsequent stimulation pulses is monitored and integrated. The integrated voltage serves as a measure for the charge mismatch. Remaining charges are compensated by matching the charge of the negative current pulse to the positive one by adjusting its stimulus amplitude. The heart of the charge balancer presented is its PI controller. Based on the design of two cross-coupled differential input pairs, the controller exhibits an extremely low transconductance of 1.5 nS. This is necessary for fulfilling the requirement of a large time constant of 8 ms, with a reasonable small on-chip capacitance of 12 pF. Further, the design was optimized for a wide linear input voltage range of 6 V, HV robustness and low-power consumption. For power saving, a shift in voltage from a maximum HV of 30 V to a LV domain of 3.3 V was implemented. The controller steers a second OTA, which interfaces the cathodic current biasing of a biphasic stimulator. With a maximal output current of ±40 nA, the balancer is capable of correcting a mismatch in cathodic stimulus up to 36% at current amplitudes up to 10 mA. The whole charge balancer consumes only 23.2 µW at a 30 V supply. Further, it is shown how the electrode parameters influence the system control behavior, and thus, stability considerations were taken. Simulation and measurement results prove the adaptability of the CB control to a wide variety of different electrodes.

6. Inter-Pulse Charge Control

The presented consequence-based charge compensation method is referred to as the Inter-Pulse Charge Control (IPCC) due to its instantaneous compensation properties in between each stimulation pulse. Thus, after the occurrence of a stimulus, the remaining electrode voltage is monitored and compared to safety limits. Exceeding these limits leads to an instantaneous charge removal. The adjustable compensation current is thereby autonomously supplied by a complementary stage. Two circuit implementations of the IPCC were developed. Both IPCC circuit solutions are presented in this chapter[7].

6.1. Conceptual Overview

The implementation of the following two IPCC versions is fundamentally different. However, both implementations are based on the same conceptual idea[8], which is presented in a simplified form in Fig. 6.1. The balancer consists of a HV compliant inverting amplifier as V_E monitoring unit that steers a class-B push-pull stage representing the compensation current driver. In its most simple form, the class-B stage consists of two MOS-transistors in common-drain configuration, stacked in a complementary pair arrangement. The timing diagram of the switch signals is depicted in Fig. 6.1. Directly after each stimulus $S_\mathrm{IPCC} = \overline{S_\mathrm{c} \cup S_\mathrm{a}}$ turns high, the monitoring of V_E starts. The compensation concept of the IPCC is demonstrated in Fig. 6.2 for an example of monophasic and imbalanced biphasic current pulses. Without charge compensation, a remaining voltage V_E rises after each stimulation, as shown in (a) and (c). Only if a predefined safety window ΔV_safe is exceeded a continuous compensation current I_IPCC is supplied. The amplitude of I_IPCC provides an upper limit and further reduces with decreasing V_E. The IPCC compensates the remaining voltage in both monophasic and biphasic stimulations, as shown in (b)

[7] In the scope of this work and chronologically conditioned, two circuit implementations of the IPCC were developed. First, the IPCC with 22 V compliance evolved and the results have been published in [13, 63] (©IEEE). However, this implementation is restricted to the supply of 22 V and is not in accordance with the quad rail methodology as described in sec. 4.2. Therefore, a second implementation of the IPCC with adaptive supply compliance was pushed ahead in form of a master's thesis of the student Utpal Kalita [82], instructed and supervised by the author of this thesis. The results led to the publication [83] (©2018, IEEE) and [86] (©2021, IEEE).

[8] The basic idea of this compensation method, as it is described in sec. 6.1, emerged from the master's thesis [15] of the author of this thesis. The idea as well as ensuing implementations, have been published in the form of a patent [84].

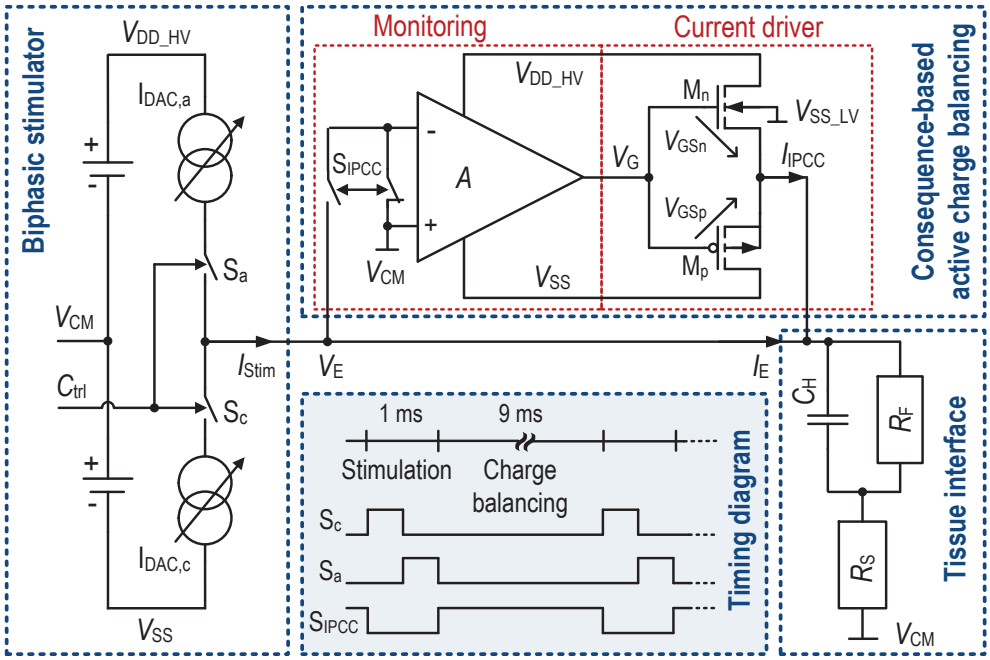


Figure 6.1.: Conceptional system overview of an IPCC active charge balancer within the stimulation setup, including an exemplary timing diagram.

and (d). In case of monophasic stimulation, the IPCC autonomously generates a counter pulse, and therefore, can be used as a complement to these types of stimulators. The IPCC becomes autonomously inactive, once V_E is reduced below the safety limits. However, S_{IPCC} stays high until the next stimulus begins, thus, being able to react to disturbances.

The main advantage of the presented IPCC is its instantaneous effectiveness with an overall simple design, as additional voltage references are dispensable in contrast to e.g. [4, 6, 9, 56]. The safety window ΔV_{safe} is autonomously defined by the gain of the amplifier A in combination with the inherent hysteresis (dead-zone) of the class-B stage. This dead-zone is provided by the threshold voltages $V_{th_{n,p}}$ of $M_{n,p}$. The amplification factor A is kept adjustable. Thus, the safety limit V_{safe} can be configured to either $\pm 50\,\mathrm{mV}$ as reported in [6], or $\pm 100\,\mathrm{mV}$ as reported in [4]. Within ΔV_{safe}, the class-B stage stays inactive and consumes no power. It turns 'on' if

$$|V_{GS_{n,p}}| \geq |V_{th_{n,p}}|\,. \tag{6.1}$$

Depending on the voltage polarity, only one transistor is conducting current at a given time, either sourcing or sinking current to or from the electrode. The conduction operation mode is saturation, since

$$|V_{DS_{n,p}}| \geq |V_{GS_{n,p}}| - |V_{th_{n,p}}| \quad \text{for} \quad |V_{GS_{n,p}}| \geq |V_{th_{n,p}}| \tag{6.2}$$

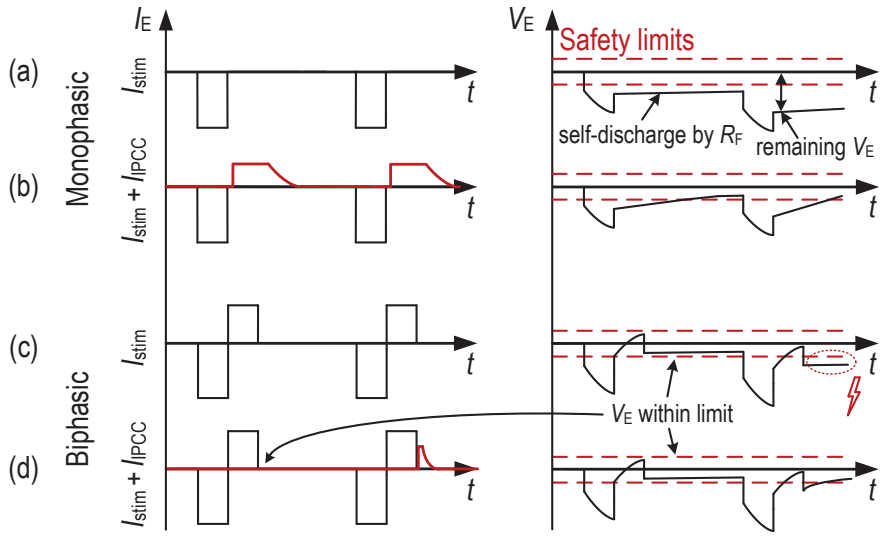


Figure 6.2.: Compensation concept of the IPCC is illustrated by the electrode current I_E and the corresponding electrode voltage V_E. (a) shows the stimulation current pulse I_{Stim} of a monophasic stimulus, and (c) of an imbalanced biphasic stimulus. (b and d) include the compensating current waveforms. Modified from [83] (©2018, IEEE).

is fulfilled. The output current I_{IPCC} increases quadratically with effective gate-source voltage

$$I_{IPCC} = \frac{\beta_{n,p}}{2} \cdot (|V_{GS_{n,p}}| - |V_{th_{n,p}}|)^2 , \tag{6.3}$$

with

$$V_{GS_{n,p}} = (-A) \cdot V_E - V_E = -V_E \cdot (A + 1) . \tag{6.4}$$

The compensating current waveform provides its highest amplitude right after the stimulus and decreases with ongoing compensation. The maximum amplitude of I_{IPCC} can be limited via the transistor's gain factor

$$\beta_{n,p} = \beta_0 \cdot (\frac{W}{L})_{n,p} . \tag{6.5}$$

An adequate dimensioning assures that I_{IPCC} is low enough to not trigger unwanted action potentials. Thus, it makes best use of the refractory period of the nerve to achieve fast settling without risking the an unwanted restimulation.

In Tab. 6.1 the working principle of the IPCC is additionally explained by a numerical example, assuming that the class-B push-pull stage provides a symmetrical HV threshold voltage $V_{th_{n,p}}$ of $\pm 6\,V$ and the safety limit V_{safe} is given by $\pm 100\,mV$. The required amplification factor can be derived from the borderline case of Eq. (6.1),

Table 6.1.: Working principle of the IPCC, assuming a symmetrical $V_{\mathrm{th_{n,p}}}$ of $\pm 6\,\mathrm{V}$ and V_{safe} of $\pm 100\,\mathrm{mV}$.

Case	V_{E}	$V_{\mathrm{G_{n,p}}}$	$V_{\mathrm{GS_{n,p}}}$	I_{IPCC}
1	$+200\,\mathrm{mV}$	$-11.8\,\mathrm{V}$	$-12\,\mathrm{V}$	$< 0\,\mathrm{A}$
2	$+100\,\mathrm{mV}$	$-5.9\,\mathrm{V}$	$-6\,\mathrm{V}$	$0\,\mathrm{A}$
3	$-100\,\mathrm{mV}$	$+5.9\,\mathrm{V}$	$+6\,\mathrm{V}$	$0\,\mathrm{A}$
4	$-200\,\mathrm{mV}$	$+11.8\,\mathrm{V}$	$+12\,\mathrm{V}$	$> 0\,\mathrm{A}$

i.e. once the remaining V_{E} equals the safety limit (case 2 and 3). Substituting V_{GS} with $V_{\mathrm{th_{n,p}}}$ in Eq. (6.4) and setting the electrode voltage V_{E} equal to the safety voltage limit V_{safe} yields the required amplification factor

$$A = \frac{-V_{\mathrm{th_{n,p}}}}{V_{\mathrm{safe}}} - 1 = -\frac{\pm 6\,\mathrm{V}}{\mp 100\,\mathrm{mV}} - 1 = 59\,. \tag{6.6}$$

In Tab. 6.1 case 1, an unbalanced stimulus pulse is applied, causing a remaining electrode voltage of $+200\,\mathrm{mV}$ exceeding the safety range. The error signal is amplified by -59 resulting in a V_{GS} of -12 V and an overdrive voltage of -6 V with respect to V_{CM}. Thus, the bottom PMOS part of the class-B stage opens and a negative current across the electrode is provoked. I_{IPCC} reduces V_{E} until the remaining voltage equals the safety value of $+100\,\mathrm{mV}$. As the class-B stage is formed by two complementary stages, a negative remaining electrode voltage would lead to positive compensation currents, increasing V_{E} accordingly. However, the safety limits are exposed to gain variations of the amplifier and threshold voltage variations of the current driver. Therefore, a safety margin was foreseen to cover all mismatch and process variations expected from simulations. Thus, the actual safety window is smaller than the predefined limits, which means, that the actual amplification factor A is chosen larger than the calculated values.

6.2. IPCC with 22 V Compliance

For LV applications, the IPCC could be implemented as shown in Fig. 6.1. However, in order to provide greater flexibility and to meet the HV requirement, the concept was further developed. A maximum compliance of 22 V in the 0.35 µm HV CMOS process was reached in this first IPCC-22 V circuit design[9]. The IPCC-22 V circuit, presented in Fig. 6.3, consists of an inverting amplifier with a closed loop gain R_2/R_1 that steers an advanced push-pull class-B stage as current driver. This chapter describes the design of the components and highlights the precautions that were taken to guarantee a HV compliance of 22 V. Further design work, to provide a

[9]The circuit and its results have been published in [63] (©2016, IEEE) and [13] (©2018, IEEE).

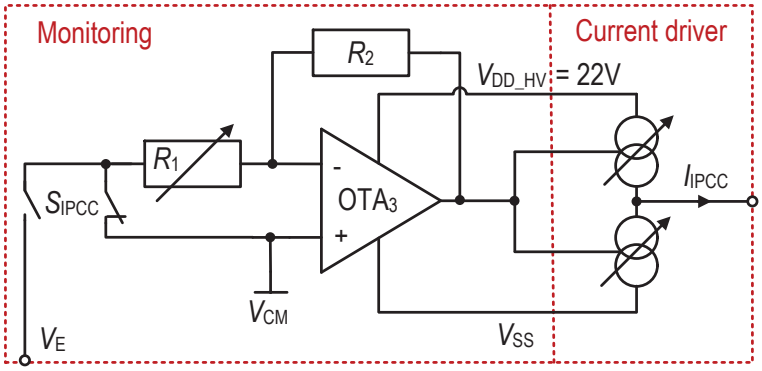


Figure 6.3.: Conceptional overview of the IPCC-22 V, consisting of an inverting amplifier with resistive feedback and a push-pull current driver.

symmetrical threshold voltage around V_{CM} and an adjustable maximum amplitude of the compensation current I_{IPCC} to predefined limits, is described. The IPCC system was tested and validated by chip measurements.

6.2.1. Operational Transconductance Amplifier

The architecture of the operational transconductance amplifier OTA_3 was implemented, consisting of a HV PMOS driven input stage with a differential current mirror load and converted to a single ended output. The unloaded OTA provides an open loop gain of 75.7 dB and UGBW of 9.8 MHz. Its characteristic was simulated and tested for process and mismatch variations by a 300 run Gaussian distributed Monte Carlo simulation, listed in Tab. 6.2.

The closed loop amplification is ideally set by the ratio of the feedback resistors R_2/R_1. The safety limit setting can be configured to either ±50 mV or ±100 mV by changing the value of R_1. Both R_1 and R_2 are polysilicon resistors of type RHP, because it provides the largest unit resistance of 10 kΩ/□ in the employed technology. The output resistance of the OTA_3 is defined by R_2. Therefore, R_2 was chosen to be 30 MΩ, as a compromise between low chip-area and large output resistance. Loaded by R_2 and further parasitic capacitances, of the actual circuit implementation, the

Table 6.2.: Characteristic values of the OTA_3 extracted from a 300 run Gaussian distributed Monte Carlo simulation.

	A_o (dB)	UGBW (MHz)	PM (°) (*)	Input offset (mV)
Mean	75.7	9.8	63.52	0.142
$\pm\sigma$	0.305	0.270	0.627	3.9

(*) loaded with 1 pF

open loop gain A_0 changes to 43.2 dB and the UGBW to 3.8 MHz. The phase margin is larger than 137 ° in the final circuit arrangement. Taking the loop error

$$\varepsilon = 1 - \frac{1}{1 + (A_0 \cdot k_{\text{loop}})^{-1}} = 1 - \frac{1}{1 + (A_0 \cdot \frac{R_1}{R_1 + R_2})^{-1}} \tag{6.7}$$

into account and choosing some margin, the gain for ±100 mV safety limit setting results to 66 with a resistance R_1 of 230 kΩ, opening the current driver at V_E of around ±70 mV. For the ±50 mV safety limit setting, the required gain to open the current driver at V_E of around ±33 mV is reached by shorting R_1 via the HV switch ($S_{1,2}$ sec. 4.4) with an on-resistance of around 4 kΩ. In this case, the feedback factor k_{loop} is decreased that much, that ε is almost one. Thus, the amplification is 144, which corresponds to the open loop gain of OTA_3.

During charge balancing, the current through R_1, provided by OTA_3, additionally decreases V_E. However, the current amplitude, which is within ±800 nA, is negligibly small compared to the compensation current I_{IPCC} of up to ±500 µA.

6.2.2. Advanced Class-B Stage

The HV transistors of the 0.35 µm HV CMOS process can withstand a maximum V_{GS} of 18 V and a maximum gate-bulk voltage V_{GB} of 22 V. Therefore, a basic class-B architecture, as shown in Fig. 6.1, could be implemented for applications of up to 18 V supply only. However, to make full use of the maximum allowed V_{GB} headroom an advanced class-B stage was introduced, shown in Fig. 6.4. Here, M_1 and M_2 are the basic transistors of the class-B output stage in common-drain configuration. In the following explanations, $R_{\text{lin1,2}}$ and $R_{\text{sd1,2}}$ are not considered yet. The 22 V compliance was reached through two precautions: First, a gate protection technique (M_{5-8}) is used, keeping V_G of $M_{1,2}$ during their inactive phase at V_{bias}, which is close to half the supply. Second, implementing transistors $M_{3,4}$ shields the source nodes $N_{1,2}$ from direct V_E variations. Otherwise, an additional switch at the output would be necessary to avoid an output current I_{IPCC} during stimulation.

The basic output current I_{IPCC} of the advanced HV class-B stage (Fig. 6.4), is now defined by the respective two transistors of the active side. Disregarding the limiting resistor $R_{\text{sd1,2}}$, the source of M_1 and M_3, as well as M_2 and M_4, are connected and the resulting current is an interplay of both transistors. At the example of the upper side with M_1 and M_3,

$$I_{\text{IPCC}} = \frac{\beta_1}{2} \cdot (V_{G1} - V_{S1} - V_{\text{th1}})^2 \tag{6.8}$$

and

$$I_{\text{IPCC}} = \frac{\beta_3}{2} \cdot (V_{S1} - V_{\text{bias}} + V_{\text{th3}})^2 \tag{6.9}$$

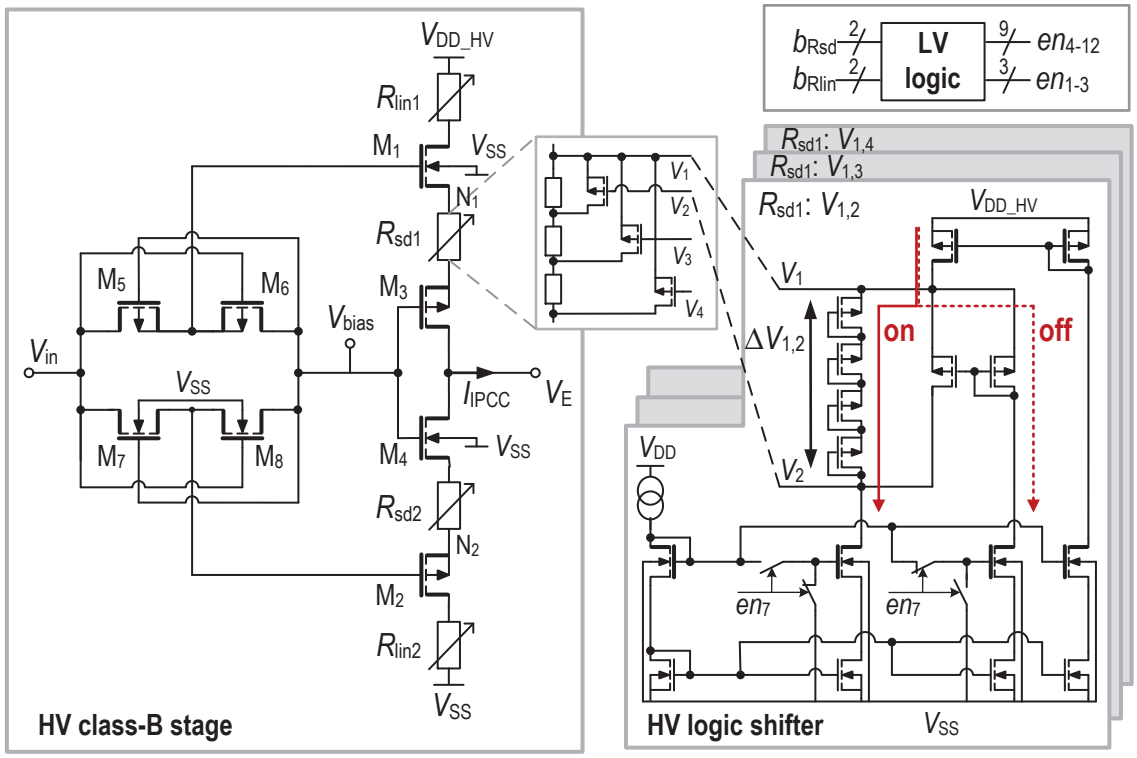


Figure 6.4.: Schematic of the implemented current driver, including the HV class-B stage with current limiting resistors $R_{sd1,2}$ and $R_{lin1,2}$, as well as the HV logic shifter, exemplarily shown for R_{sd1} [13] (©2018, IEEE).

must hold. With the assumption that V_{bias} is fixed to around V_{CM}, which is used as virtual ground, Eq. (6.9) can be solved for V_{S1} and substituted in Eq. (6.8). The gate voltages $V_{G1,2}$ of the active side, changes proportionally with V_E, which finally leads to a current equation

$$I_{IPCC} = \frac{k}{2} \cdot \left(|V_E| \cdot \frac{R_2}{R_1} - (V_{th1,4} + |V_{th3,2}|) \right)^2 . \tag{6.10}$$

The factor k scales the current according to

$$k = \beta_{1,3} \cdot \beta_{2,4} \cdot \frac{(\sqrt{\beta_{1,3}} \pm \sqrt{\beta_{2,4}})^2}{(\beta_{1,3} - \beta_{2,4})^2} . \tag{6.11}$$

Similar to the simple class-B architecture shown in Fig. 6.1, I_{IPCC} of the advanced HV class-B stage still changes quadratically with V_E, however, with V_{GS} of Eq. (6.4) decreased by one V_E. The threshold to open the stage is now increased to the sum of both the threshold voltages.

Differences in the bulk connections of the NMOS and PMOS transistors result in an asymmetrical threshold voltage range of the upper and lower class-B stage, and thus, in an asymmetric safety window ΔV_{safe}. However, this advanced class-B stage

provides the possibility to bias the gates of transistor M_3 and M_4. Thus, the overall upper and lower activation threshold is symmetrized around V_{CM} by slightly adjusting V_{bias} to

$$V_{bias} = V_{CM} - \frac{(V_{th1} + |V_{th3}|) - (|V_{th2}| + V_{th4})}{2} . \tag{6.12}$$

The threshold voltages V_{th1-4} were determined by simulations and V_{bias} resulted to 1.35 V above V_{CM}. However, to allow calibration during measurements, the biasing voltage of this prototype is generated off-chip.

For charge compensation a flat slope and low compensation amplitudes are preferred, since both influence the sensitivity of neurons to trigger action potentials [85]. The maximum allowed compensation current amplitude depends on the stimulation site and application. Therefore, a versatile system with high flexibility is desired. The upper output current limit is set to a predefined limit by choosing adequate design dimensions. In this implementation the upper limit is set to ±500 µA. Further, two methods for varying the slope and maximum amplitude of I_{IPCC} were implemented (Fig. 6.4): The current intensity can be limited either by increasing a resistance $R_{sd1,2}$ inducing source degeneration, or by increasing $R_{lin1,2}$, reducing the drain voltages, and thus, forcing $M_{1,2}$ earlier into the linear region (earlier 'pinch off'). The maximum compensation amplitude is configurable to predefined limits between ±150 µA and ±500 µA by a 2-bit LV signal b_{Rsd} and b_{Rlin}, respectively. Each resistor consists of three sub-resistances, like exemplary illustrated in Fig. 6.4 for R_{sd1}. Beside R_{lin2} all resistors are exposed to a HV environment. Thus, a HV logic shifter is required, shifting the LV digital control signals en_{4-12} into the HV domain. The concept of the HV logic shifter was deduced from the HV switch presented in sec. 4.4. In the 'on' condition a current of 10 nA is directed through a series of diode connected transistors, providing a sufficient $\Delta V_{1,2}$ to open the switching transistor, thus, shortening one sub-resistance. In the 'off' state the same 10 nA are being directed through the second branch, actively pulling V_1 towards V_2 via the parallel current mirror configuration, closing the switching transistor.

6.2.3. Measurement Results

All measurements were performed with the chip shown in Fig. 6.5. Its active area, comprising numbers 1 to 6, is less than 0.26 mm^2. With OTA_1 being the main active device in the monitoring steady state, the IPCC circuit consumes only 37.1 µW at a 22 V supply, see Tab. 6.3. However, if needed, the class-B stage is capable of delivering an output power as high as 11 mW.

The measured characteristics of I_{IPCC} over V_E are shown in Fig. 6.6. Within the dead-zone of the IPCC no current is released onto the electrode. In the upper two graphs, the mean of the dead-zone corresponds to the safety window of ±50 mV. In a 300 run Gaussian distributed Monte Carlo simulation, the mean is ±33 mV around

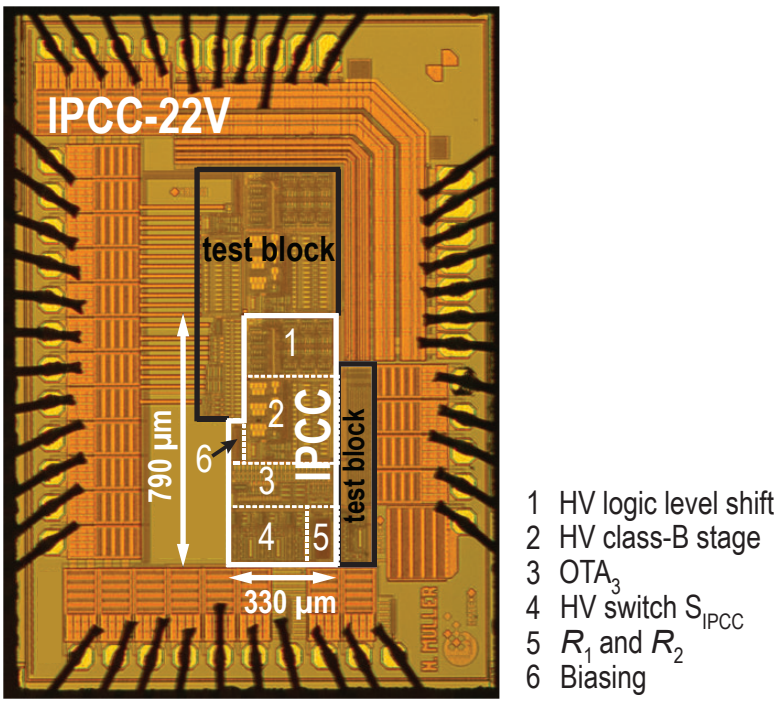


Figure 6.5.: Micrograph of the IPCC with a fixed 22 V compliance. Modified from [13] (©2018, IEEE).

V_{CM} with σ uncertainty below 4.6 mV. The mean of the dead-zone that corresponds to the safety window of ±100 mV (Fig. 6.6 lower graphs), is ±70 mV around V_{CM} with σ uncertainty below 4.7 mV. All graphs in Fig. 6.6 show that once V_E exceeds the dead-zone, the current increases quadratically. The solid black line in all graphs show I_{IPCC} without resistive current limitations. It reaches a maximum of about ±500 µA. In this prototype, the same maximum current limits of ±150 µA, ±300 µA, and ±400 µA were chosen to show that the same limits can be generated in two ways, via R_{lin} or R_{sd}. A combination of the latter would also be possible to further limit the current. Here, however, the two limiting methods were only used separately to illustrate the different limiting effects. The drain current induced voltage drop over R_{lin} (Fig. 6.6(a)) decreases the dynamic range and limits the maximum output current. In contrast, increasing R_{sd} (Fig. 6.6(b)) limits the current by flattening the output slope of I_{IPCC}, while keeping the dynamic range constant.

System verification of the IPCC were performed using an early version of the analog front-end of the stimulator presented in sec. 4.3, controlled by an off-chip FPGA. An electrode equivalent model with C_H of 0.1 µF, R_F of 500 kΩ, and R_S of 1 kΩ was chosen. The measured CB response of the IPCC is presented in Fig. 6.7 for two different current limits, resulting in different amplitudes, slopes and settling times of I_{IPCC}. The safety limit is set to ±50 mV. The green line shows the compensation with I_{IPCC} limited to around 500 µA, and the red line with I_{IPCC} restricted to a maximum amplitude of around 150 µA. The stimulation pulse of Fig. 6.7(a)

Table 6.3.: Power consumption of the IPCC-22 V in its monitoring steady state, listed by components.

Main components		OTA_3	Class-B stage	HV logic shifters	$3 \cdot S_{IPCC}$	Basing
Supply voltage	V	22	22	22	22	3.3
Current consumption	µA	1.22	0	0.15	0.06	0.41
Simulated total power	µW			34.1		
Measured total power (incl. 1 µA test pin)	µW			37.1		

illustrates the case of cathodic-first stimulation, exhibiting a 30% surplus in negative charges, whereas Fig. 6.7(b) proves the concept in opposite direction, with a 30% surplus in positive charges and anodic first stimulation. Fig. 6.7(c) shows a monophasic cathodic stimulus that requires 100% stimuli mismatch compensation by autonomously generating the counter pulse. All three current pulses Fig. 6.7(a-c) show peak artifacts. These are subject to the over and undershoots of an early prototype of the stimulator front-end, and the rough switching of the simplified measurement setup, where each time the complete biasing of the stimulator front-end is switched on and off. A statement and more details on the switching effects within the front-end stimulator are described in sec. 4.3.2. However, these artifacts have no influence on the IPCC efficacy and system verification. The black lines of V_E in Fig. 6.7 trace the case without charge balancing. A remaining V_E of around 2 V was developed already after the first stimulus (Fig. 6.7 (a) and (b)). Using IPCC, V_E was reduced into the safe window due to the autonomous supply of compensation current I_{IPCC}. The lower the current restrictions, the faster is the compensation. Once V_E enters the safe region, the IPCC becomes automatically inactive. As a special feature, the IPCC can be used as a complement to monophasic stimulators, since it replaces the missing biphasic pulse of Fig. 6.7(c) and reaches full charge compensation with respect to the safety limits.

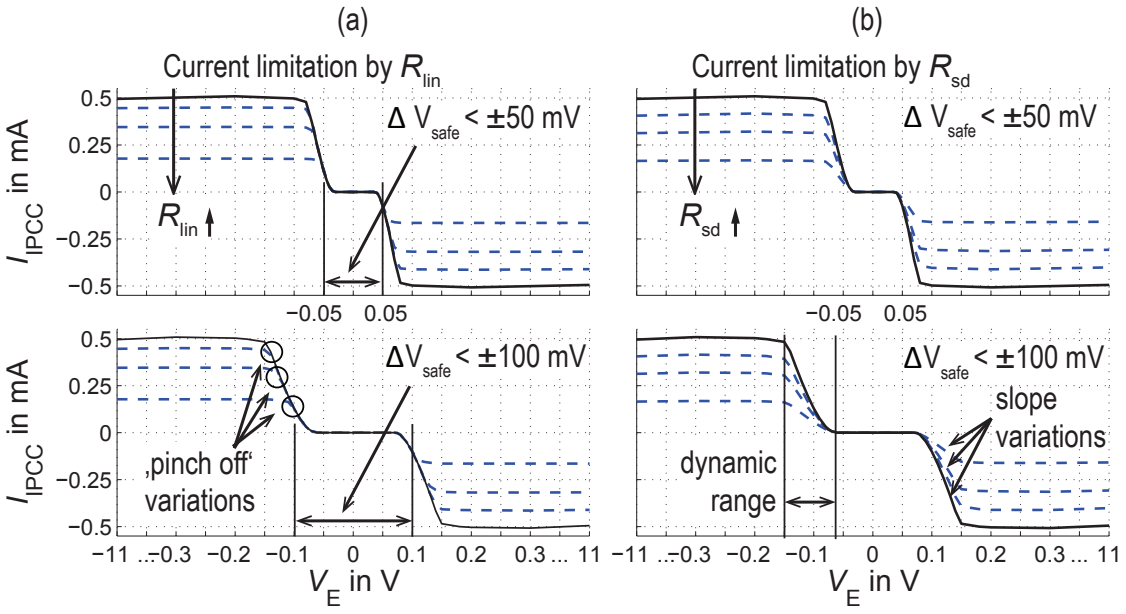


Figure 6.6.: Measured characteristics of the IPCC-22 V with a safety window of ±50 mV in the upper and ±100 mV in the lower graphs, showing the influence on I_{IPCC}, when increasing (a) R_{lin}, and (b) R_{sd} [13] (©2018, IEEE).

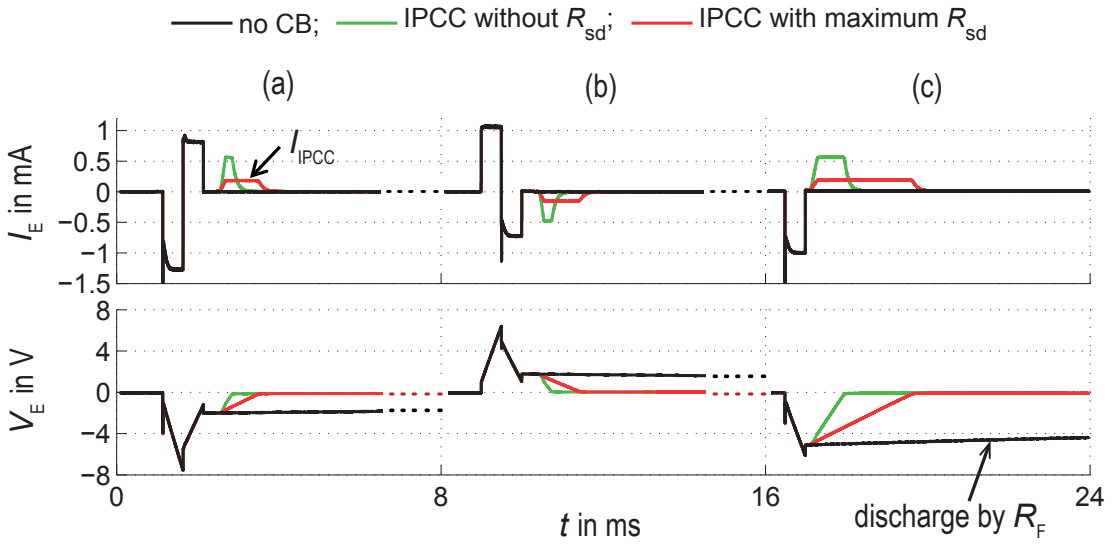


Figure 6.7.: Measured system results of the IPCC-22 V for compensation currents I_{IPCC} limited to around ±500 µA (green) and to around ±150 µA (red), using an electrode equivalent model with C_H of 0.1 µF, R_F of 500 kΩ, and R_S of 1 kΩ. An intended mismatch is introduced (a) in the cathodic phase, (b) in the anodic phase, and (c) by applying a monophasic stimulus. Adjusted from [13] (©2018, IEEE).

6.3. IPCC with Adaptive Supply Compliance

In contrast to the IPCC-22 V that is fixed to a 22 V supply due to technological limits, this second circuit design[10], the IPCC with adaptive supply (IPCC-AS), overcomes these limitations by splitting the biasing of the class-B stage. The circuit design conforms to the quad-rail concept sec. 4.2, and thus, becomes configurable with supply voltages from 3.3 V to 38 V. This IPCC-AS implementation consists of a fully differential operational transconductance amplifier (FDOTA) as HV monitoring unit and a class-B stage with four biasing voltages as current driver for charge compensation. As illustrated in Fig. 6.8, the FDOTA contains four blocks: the differential input stage, an intermediate level translator (ILT) stage, and the LV and HV output stages. In an open loop configuration, the FDOTA compares V_{E} to V_{CM} and enhances the differential input voltage. The advantage over an external feedback [13] is its high input impedance, i.e. a DC decoupling between the FDOTA as charge sensor and the tissue interface. The FDOTA provides two differential output pairs $V_{\mathrm{HV+}}$, $V_{\mathrm{HV\text{-}}}$ and $V_{\mathrm{LV+}}$, $V_{\mathrm{LV\text{-}}}$. Both are compatible with the $\triangle \mathrm{V}_{\mathrm{LV}}$ quad-rail domains and steer the upper and lower current driver stages, respectively. Thus, in contrast to the previous advanced class-B stage (Fig. 6.4), the biasing of the push and pull part of the current driver is now split and kept within the $\triangle \mathrm{V}_{\mathrm{LV}}$ domains. This is advantageous in terms of die area and symmetry of the threshold voltages, since LV components for the lower but also the upper current driver can be used exclusively. Additionally, the implemented LV transistors provide a triple well process, which was not available for the HV transistors implemented in the advanced class-B stage, and therefore, lower threshold voltages can be achieved.

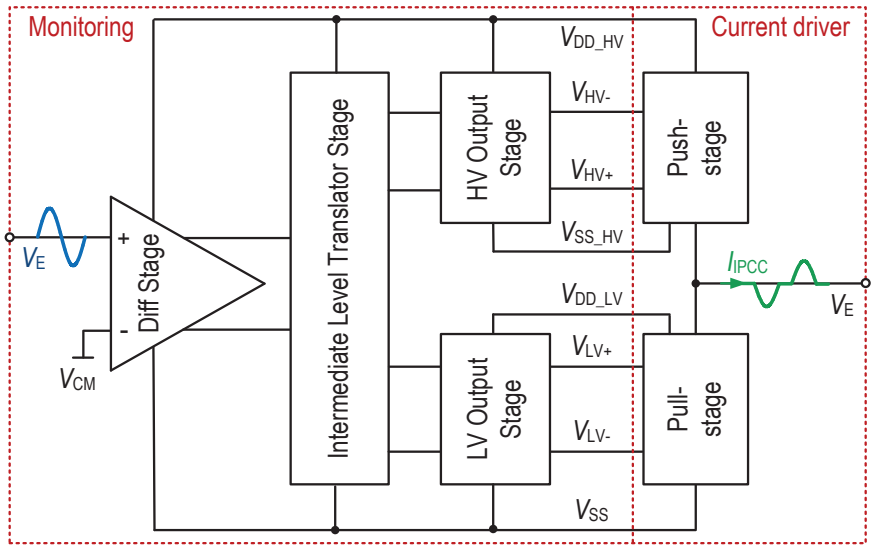


Figure 6.8.: Block diagram of the four stages of the FDOTA as monitoring circuit, and the push-pull class-B current driver.

[10]The circuit and its results have been published in [83] (©2018, IEEE) and [86] (©2021, IEEE).

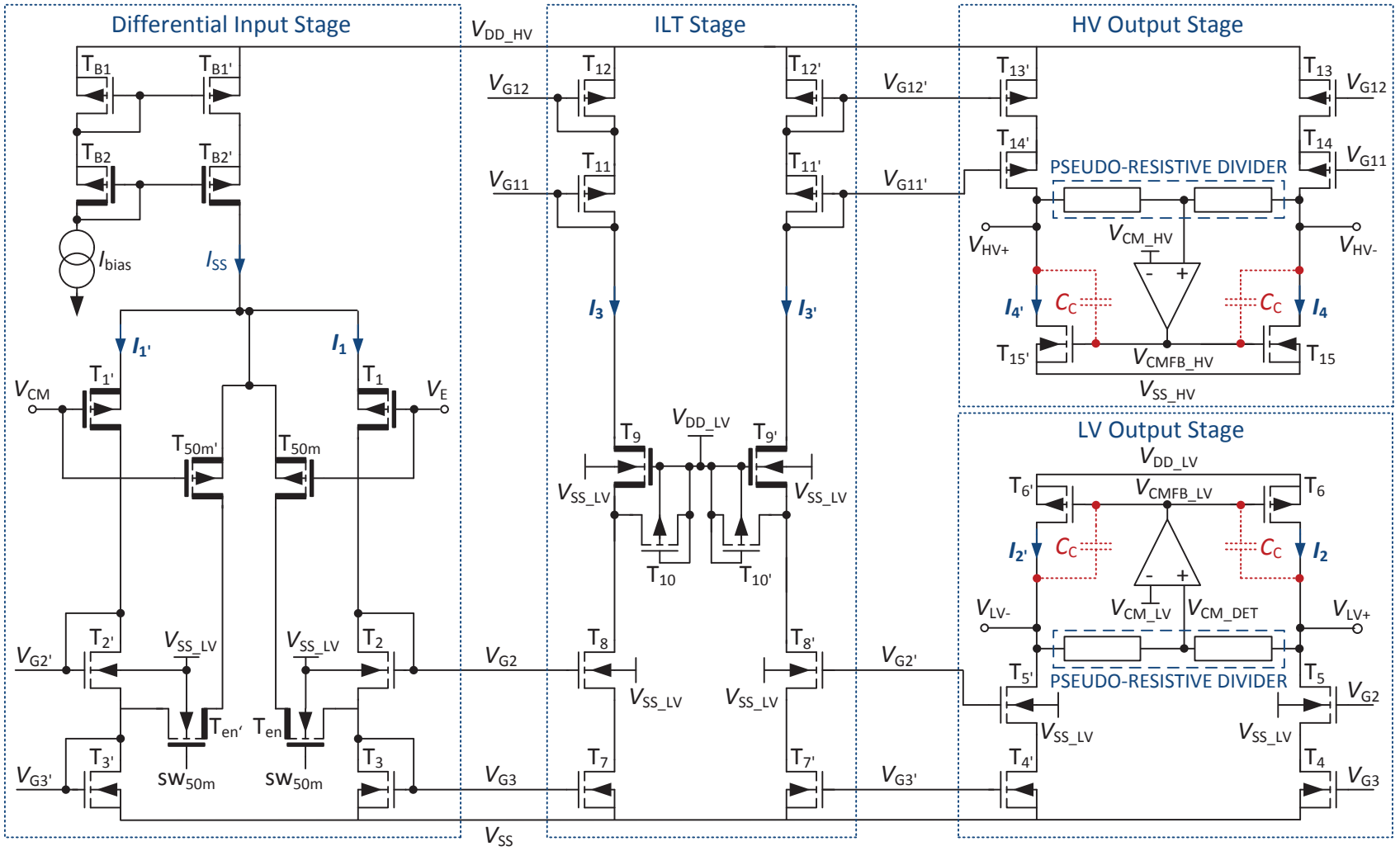


Figure 6.9.: Transistor level implementation of the four stages of the FDOTA, including CMFB loop of the output stages and Miller compensation cap C_C [86] (©2021, IEEE).

6.3.1. Fully Differential Operational Transconductance Amplifier

The transistor level implementation of the FDOTA is shown in Fig. 6.9. The HV transistors $T_{1,1'}$ represent the basic input pair of the differential input stage, where V_E and V_{CM} are applied. The FDOTA allows switching between the two safety limit values (±50 mV, ±100 mV) by changing the input transconductance $g_{m,in}$ of the differential input stage, and thus, the FDOTA's open loop gain. Therefore, two additional input transistors $T_{50m,50m'}$ were introduced in parallel to $T_{1,1'}$, increasing $g_{m,in}$. The switching is carried out by $T_{en,en'}$ that are connected to the sources of $T_{2,2'}$ instead of their drains to lower the source voltage of $T_{en,en'}$. This ensures that a signal sw_{50m} of 3.3 V is sufficiently high to activate $T_{en,en'}$. Thus, the open loop gain of around 23.8 for ±100 mV is increased to around 47.6 for ±50 mV safety limit. Simulated and measured results of the FDOTA's overall transconductance $G_{m,FDOTA}$ are compared in Fig. 6.10 and show a good match. $G_{m,FDOTA}$ is around 1.55 µS for the ±50 mV safety limit setting, and around 0.84 µS for the ±100 mV safety limit setting.

The differential input signal is directly mirrored by $T_{2,2'}$ and $T_{3,3'}$ to $T_{4,4'}$ and $T_{5,5'}$ into the LV output stage, that operates in the lower $\triangle V_{LV}$ subrange. However, the translation of the differential input signal into the upper $\triangle V_{LV}$ subrange requires a level shift. The differential current is therefore mirrored into the ILT stage by $T_{2,2'}$, $T_{3,3'}$ and $T_{7,7'}$, $T_{8,8'}$. The ILT stage operates in the overall HV environment $\sum V_{HV}$. In contrast to the LV transistors $T_{2,2'}$ of the differential input stage, the drains of $T_{8,8'}$ are not diode connected. Hence, these must be protected from HV. For that purpose, two HV transistors $T_{9,9'}$ with their gates fixed to V_{DD_LV} were introduced. In saturation, their gate-source voltages prevent the drains of $T_{8,8'}$ to exceed V_{DD_LV}. However, in a zero current condition of I_3 or $I_{3'}$ the drain of T_8 or $T_{8'}$ is exposed to a high ohmic node, and an additional protection scheme is necessary: two diode-connected PMOS transistors $T_{10,10'}$ were placed between the sources and gates of $T_{9,9'}$, clamping the drain of $T_{8,8'}$ to a maximum of V_{DD_LV}. The LV and HV output stages were designed symmetrically. Due to the low open loop gain requirement of the FDOTA, the load transistors $T_{6,6'}$, $T_{15,15'}$ are biased in triode region, which decreases the output resistance. Their gates are biased by a common mode feedback (CMFB) circuit, controlling the output common mode to half the $\triangle V_{LV}$ range.

6.3.2. CMFB Circuit

The proposed IPCC-AS implementation requires the full output swing of the FDOTA of 3.3 V to fully activate the current driver. Therefore, within the output stages of Fig. 6.9, a resistive voltage divider is used to detect the actual common mode voltage V_{CM_DET}. V_{CM_DET} is then compared to the wanted common mode voltage V_{CM_LV} and increased by the positive gain of a single-stage differential amplifier. The HV CMFB design is analogous to the LV one, however, with an inverted

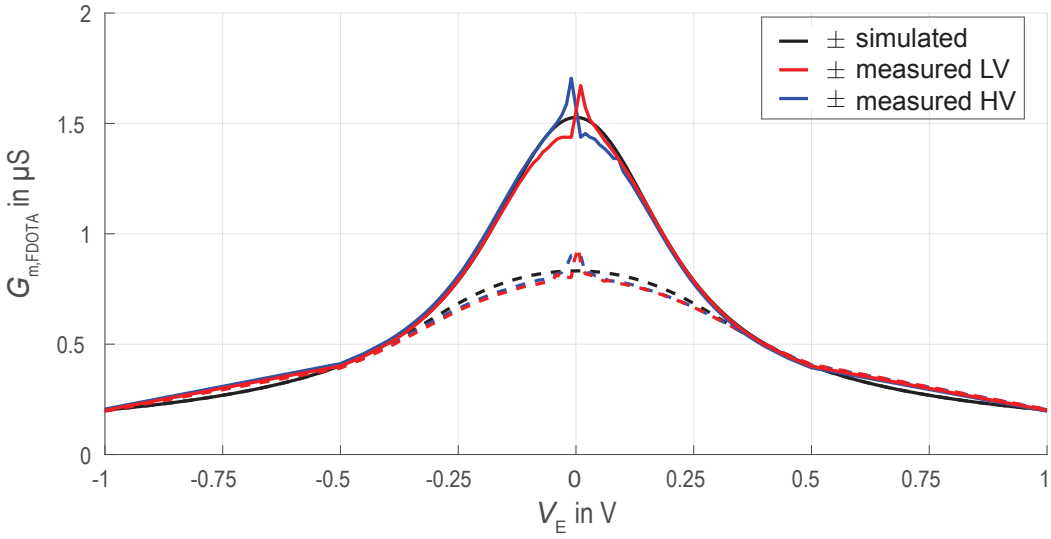


Figure 6.10.: The simulated transconductance of the differential input stage is compared to the transconductance measured at the LV and HV outputs of the FDOTA. The solid lines show $G_{\mathrm{m,FDOTA}}$ at $\triangle \mathrm{V}_{\mathrm{safe}}$ of $\pm 50\,\mathrm{mV}$ and the dashed ones at $\triangle \mathrm{V}_{\mathrm{safe}}$ of $\pm 100\,\mathrm{mV}$ [86] (©2021, IEEE).

architecture and with isolated transistor types due to the increased bulk-substrate requirement of the HV output stage.

The implementation of the high ohmic voltage divider is shown in Fig. 6.11. Four pseudo-resistor pairs [80] were used, which can provide resistances in the giga-ohm range at a small die area. Good symmetry can be achieved by connecting the source terminals of each pseudo-resistor PMOS pair P and P′ back to back. The bulk of each transistor is connected to its drain terminal. The transistors operate in subthreshold region, providing a very high linear resistance across their drain-source terminals. The resistance is tuned by the common drain transistor T_{SF} that defines V_{SG} according to its dimension and biasing current of 20 nA. Derived from [80], the resistance for one transistor can be formulated as

$$R_{\mathrm{SD}} = \frac{1}{G_{\mathrm{SD}}} = \frac{L}{2n\beta_0 W V_{\mathrm{T}} G_{\mathrm{SD0}}} e^{\frac{|V_{\mathrm{th}}|-V_{\mathrm{SG}}}{nV_{\mathrm{T}}}}, \tag{6.13}$$

where G_{SD0} is the output conductance at zero source-drain voltage, V_{T} is the thermal voltage (typically around 25 mV at room temperature) and n is the subthreshold slope factor of the PMOS device (typically in the range of 1-2). According to Eq. (6.13), the resistance can be tuned by the source-gate voltage and the transistor dimensions. A resistance value of around 600 MΩ was seen as an adequate choice, since it is much higher than the load resistance of the FDOTA and ensures a current less than 6 nA at full output voltage swing. In addition to the four symmetrical pseudo-resistor pairs eight polysilicon diodes D_{1-8} were introduced as shown in Fig. 6.11, to protect the pseudo-resistors from exceeding the maximum allowed source-bulk voltage.

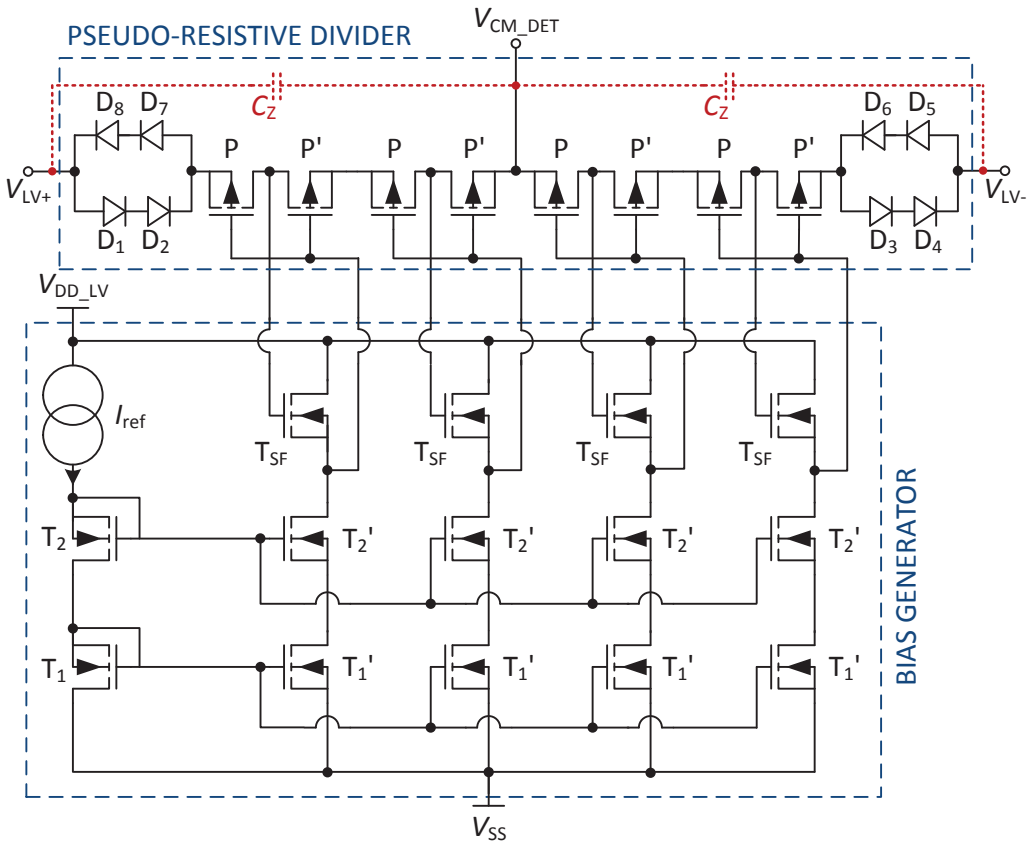


Figure 6.11.: Schematic of the proposed pseudo-resistive divider with bias-generator and capacitance C_Z for the compensation zero [86] (©2021, IEEE).

The CMFB amplifier together with the output stage of the FDOTA represents a two-stage amplifier. For stability reasons the dominant pole that originates from the CMFB amplifier, was further separated by using Miller compensation. Therefore, the two capacitances C_C of 800 fF were introduced between the gate and the drain of the load transistors $T_{6,6'}$, as shown in Fig. 6.9. A second pole arises at the output of the FDOTA, where the pseudo-resistors are connected, and is compensated by inducing a zero via the capacitors C_Z of 400 fF, as shown in Fig. 6.11. A third pole appears at the input of the CMFB amplifier. The phase margin of the LV and HV CMFB loops were finally optimized to 52° with a unity-gain frequency of 13 kHz and 36° with a unity-gain frequency of 16.4 kHz, respectively. The simulated bode plots are presented in Fig. 6.12. The small difference in phase margin of the LV and HV CMFB loops is mainly due to the difference in capacitance of the upper and lower current driver halves.

The simulated layout-extracted results of the FDOTA's output swing at a 40 V supply and for both safety limit settings are presented in Fig. 6.13. The output voltages V_{LV+} and V_{LV-}, as well as V_{HV-} and V_{HV+}, are controlled within their $\triangle V_{LV}$ subrange of 3.3 V. The threshold of 2.2 V, that turns the current driver on, is reached

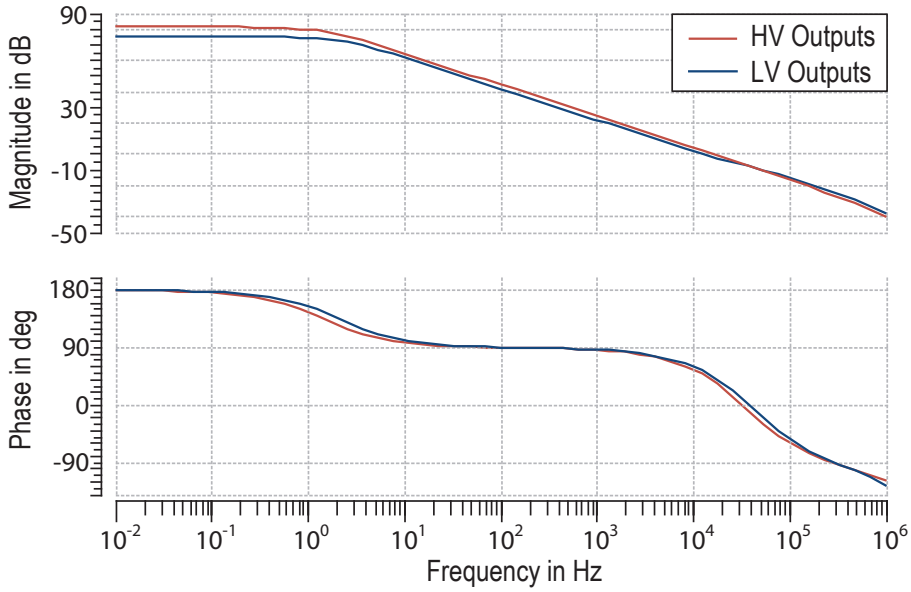


Figure 6.12.: Simulated frequency response of the LV and HV CMFB loop [86] (©2021, IEEE).

at around the safety limits. The worst case Monte Carlo (wc MC) results of 300 runs are included in Fig. 6.13. The 3σ results at the safety limits are most crucial for the switching of the current driver and show an acceptable deviation.

6.3.3. Split-Bias Class-B Stage

The current driver, shown in Fig. 6.14, is based on the class-B concept of the previous IPCC design sec. 6.2.2. The concept was modified by splitting the biasing of the intermediate transistors $T_{3,4}$ and translating it into the quad-rail $\triangle V_{LV}$ domains. The gates of all four transistors are supplied by the outputs of the FDOTA. In this way, it was guaranteed that the difference between the gate voltages of upper and lower current driver does not exceed the $\triangle V_{LV}$ subranges. The compensation current characteristic is thus independent of the overall HV environment $\sum V_{HV}$. Another advantage of the presented current driver is that the bulk of the isolated LV transistor T_1 can be directly connected to its source, or as shown here to V_{SS_HV}. Thus, the threshold voltages of both stages are almost equal. Additionally, the 22 V supply voltage restriction of sec. 6.2.2 is increased to 40 V as shown in simulations in Fig. 6.13, now restricted by the maximum allowed gate-drain voltage of T_3 and T_4 in the employed 0.35 µm HV process technology.

The working principle is illustrated for a varying V_E, highlighted in blue in Fig. 6.14. If V_E increases relative to V_{CM}, the voltages of the gates of $T_{1,2}$ decrease, while those of the gates of $T_{3,4}$ increase. This results in the activation of the lower half, provided that the overhead voltage surpasses the sum of the threshold voltages of

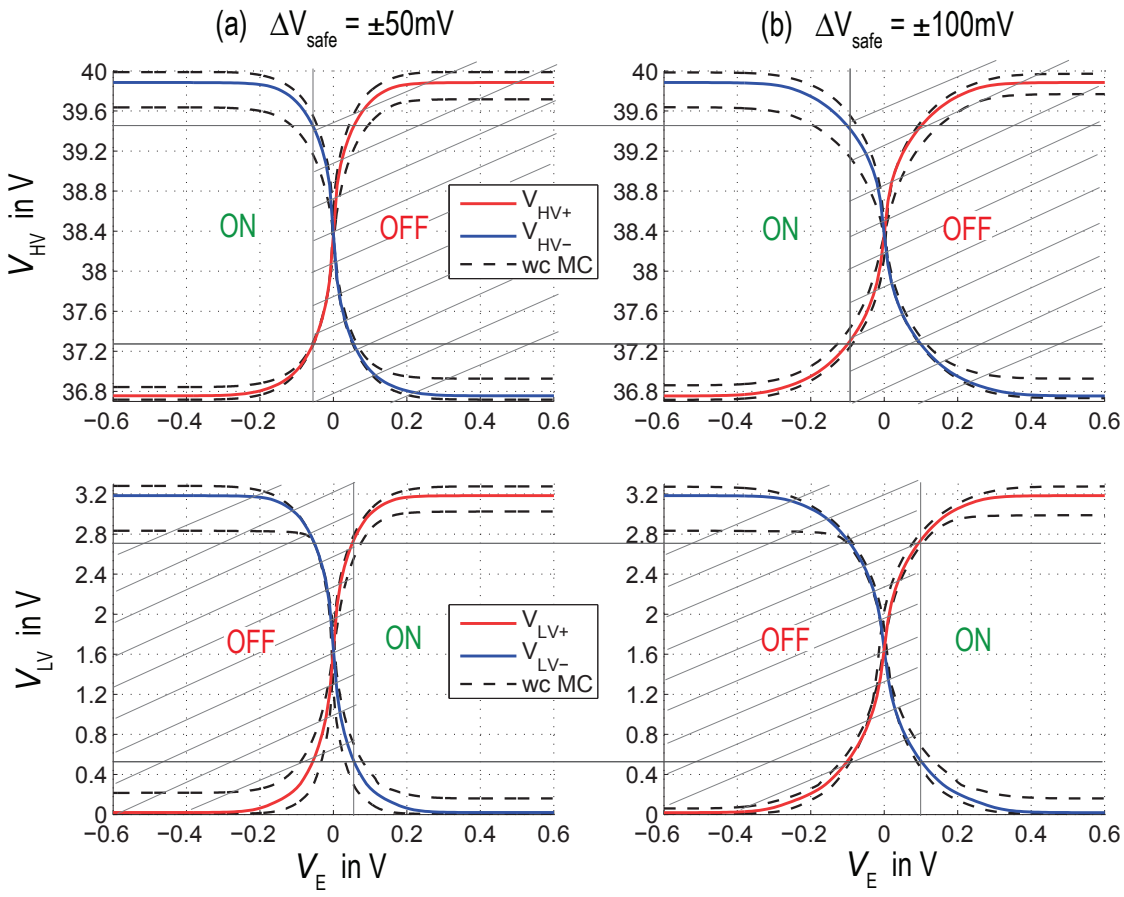


Figure 6.13.: Simulated layout-extracted output characteristic of the FDOTA with respect to changes in V_E for (a) ±50 mV and (b) ±100 mV safety limit, including worst case Monte Carlo results [83] (©2018, IEEE).

$\mathrm{T}_{2,4}$. In this case, the circuit sinks the current I_IPCC, compensating excess charges and decreasing V_E again. In the opposite case, when V_E falls below the safety limit, the upper half is activated, sourcing current into the tissue to increase V_E. I_IPCC changes quadratically with V_E defined by

$$I_\mathrm{IPCC} = \frac{k}{2} \cdot \left(|V_\mathrm{E}| \cdot A_\mathrm{FDOTA} - (V_\mathrm{th1,4} + |V_\mathrm{th3,2}|)\right)^2 , \tag{6.14}$$

scaled by k as in Eq. (6.11), according to the transistor dimensions of $\mathrm{T}_{1,3}$ and $\mathrm{T}_{2,4}$. The intrinsic dead-zone defines the safety limit, beyond which I_IPCC is pushed into or pulled out of the nervous tissue. The allowed maximum I_IPCC depends on the stimulation site and application. Two methods for current amplitude limitation have been investigated and proved by chip measurements in sec. 6.2.2. The method that limits the current amplitude to a predefined value without affecting the compensation gain was also incorporated in this improved current driver design. Therefore, two configurable resistors $R_\mathrm{lin1,2}$ were introduced between the outer supply rails and

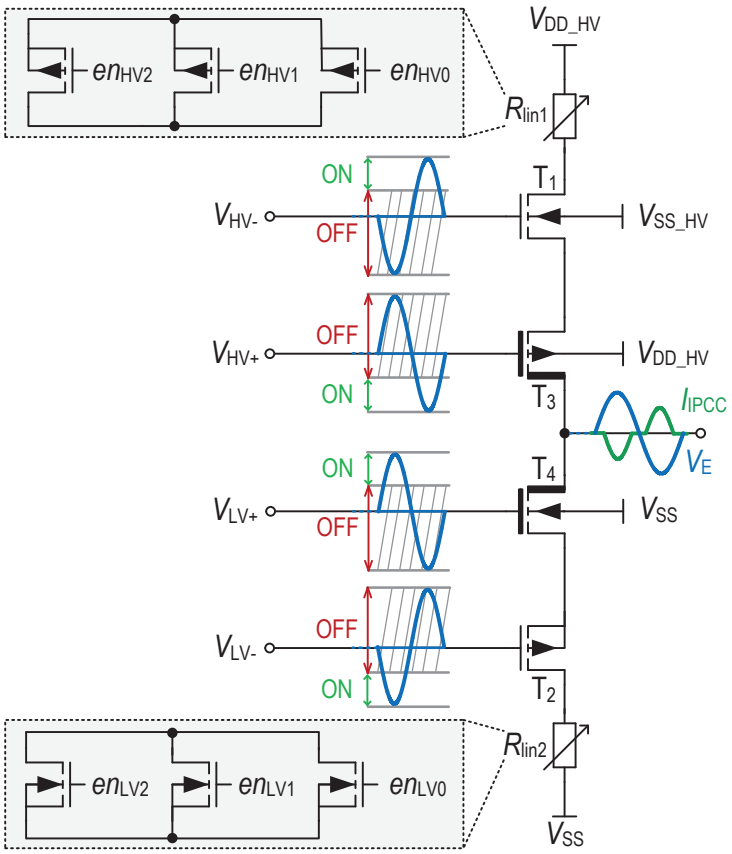


Figure 6.14.: Working principle of the current driver with variable resistances $R_{\mathrm{lin1,2}}$ for maximum current amplitude selection. Modified from [83] (©2018, IEEE).

the drain of $T_{1,2}$. As an improvement to sec. 6.2.2, the configurable resistances $R_{\mathrm{lin1,2}}$ were implemented by three transistors each, which simultaneously serve as switches, to select among three maximum current amplitudes. The HV logic level shifters were taken from the previous design. The three maximum current amplitudes of I_{IPCC} are ±500 µA, ±300 µA and ±200 µA.

6.3.4. Simulated System Results

The performance of the IPCC system was simulated using an ideal current source and an electrode-electrolyte tissue interface model with C_{H} of 0.1 µF, R_{F} of 100 kΩ and R_{S} of 1 kΩ. The results of Fig. 6.15 verify the same charge balancing efficacy for the minimum and maximum allowed supply of 6.6 and 40 V. First, an unbalanced biphasic pulse of 2 mA cathodic and 1.5 mA anodic amplitude was applied, causing a remaining voltage V_{E} of −122 mV with respect to V_{CM}. This voltage is slightly larger than the defined safety limit of ±100 mV, resulting in a small compensation current I_{CB} with a peak amplitude of 123 µA. I_{IPCC} decreases gradually with decreasing

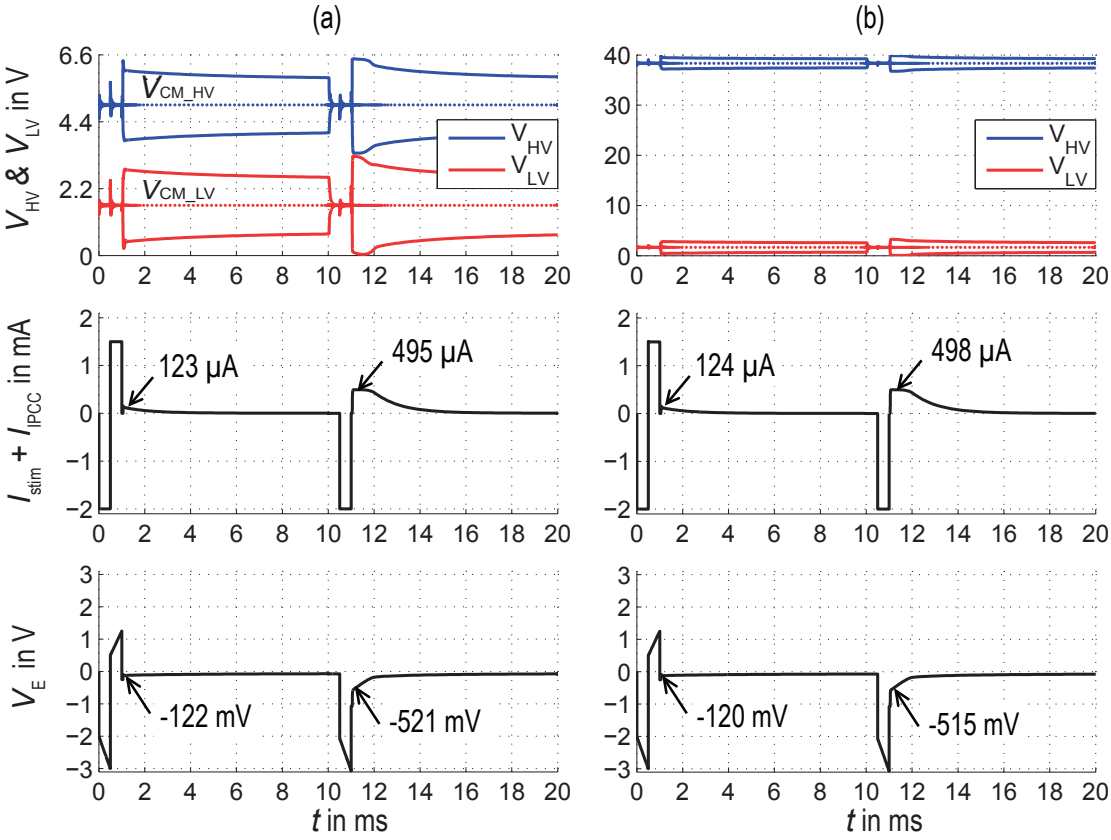


Figure 6.15.: Simulated layout-extracted IPCC results for a safety limit of ±100 mV with a supply of (a) 6.6 V, and (b) 40 V [83] (©2018, IEEE).

V_E and reaches the safety limit within 1 ms. Second, to illustrate a compensation scenario in the opposite direction and of larger mismatch, a monophasic cathodic stimulus of 2 mA amplitude was applied. A large remaining V_E of −521 mV activates the maximum I_{CB} that is limited in this setup to around 500 µA. The safety limit is reached within 2.8 ms under nominal conditions, and within 4.9 ms in a worst case MC scenario.

6.3.5. Measurement Results

The circuit was manufactured in a 0.35 µm HV CMOS process and verified by chip measurements. The chip micrograph is shown in Fig. 6.16. The die area is 0.208 mm^2. The simulated current consumption of each component is listed in Tab. 6.4. In the steady state, with the FDOTA being the only main active device, the power consumption of the circuit (pads excluded) is as low as 6.3 µW at a 3.3 V supply. Even at a HV supply of 38 V the power consumption is 24.6 µW only, which is the smallest compared to state-of-the-art (Tab. 6.5). However, if needed, the system is capable of delivering an output power as high as 19 mW.

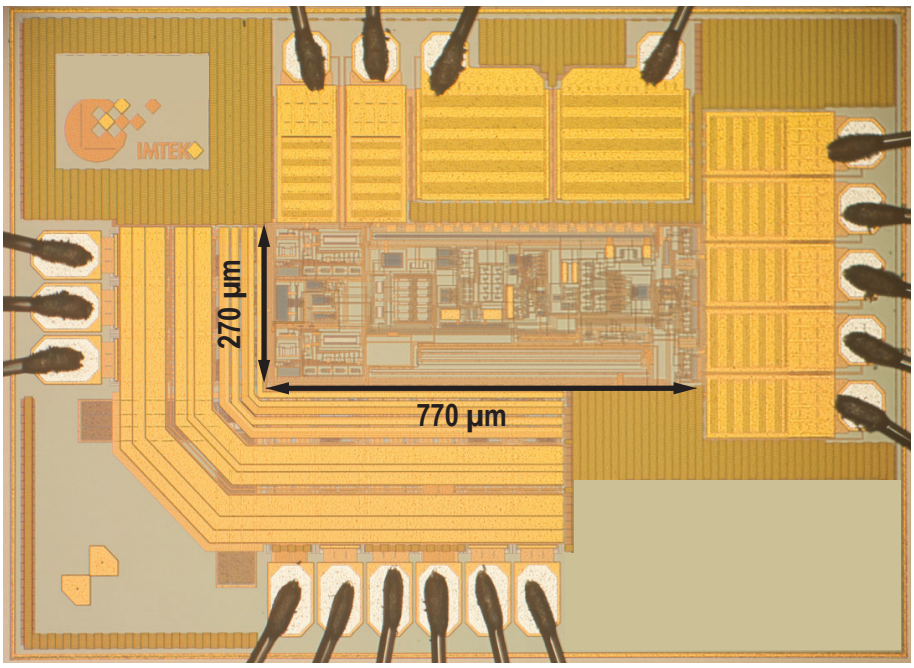


Figure 6.16.: Chip micrograph of the IPCC with adaptive supply compliance [86] (©2021, IEEE).

Table 6.4.: Simulated power consumption of the IPCC-AS in its monitoring steady state, listed by components.

Main components		FDOTA Input & ILT stage	FDOTA Output stages	CMFB circuit	Class-B stage	HV logic shifter	$2 \cdot S_{\mathrm{IPCC}}$
Supply voltage	V	3.3 to 38	3.3	3.3	3.3 to 38	3.3 to 38	3.3 to 38
Current consumption	nA	408	426	220	0	30	40
Simulated total power	µW			6.3 to 24.6 (15.8 at 22 V)			

The measured compensation current I_{IPCC} characteristic is shown for different $R_{\mathrm{lin1,2}}$ settings and safety limits in Fig. 6.17(a) and (b). Within the safety limits, where $\mathrm{T}_{1\text{-}4}$ are turned off, no current is released into the tissue interface. Once the safety limits are exceeded, the current increases quadratically with the overdrive voltage. The three current limitation settings of around ±500 µA, ±300 µA and ±200 µA are reached by increasing $R_{\mathrm{lin1,2}}$. The safety limits are adjustable to ±100 mV illustrated by the solid lines and ±50 mV illustrated by the dashed ones. The safety limits are exposed to open-loop gain variations of the FDOTA and threshold voltage variations of the current driver. Therefore, a safety margin was foreseen to cover all mismatch

and process variations expected from simulations. Thus, the actual safety window is smaller than the defined limits, as it is visible in Fig. 6.17(c). The measured chip exhibits an asymmetric safety limit of around +13 mV with respect to V_{CM}. However, the dead-zone is still within the predefined range of ±100 mV.

The characteristic curves at different supply voltages can be compared between (a), (b) and (c). Results of (a) were measured at a minimum supply of 3.3 V (±1.65 V with respect to V_{CM}), (b) at a maximum supply of 38 V (±19 V with respect to V_{CM}), and (c) at an asymmetric supply of +19 V/-1.65 V and +1.65 V/-19 V with respect to V_{CM}. A supply range displacement of +36.35 V/-1.65 V and +1.65 V/-36.35 V is not possible, due to the maximal allowed value of ±20 V between the gate and source of the FDOTA input transistors. Considering the differential implementation of the input pairs, +21.5 V/-1.65 V and +1.65 V/-21.5 V would be the maximum asymmetric supply displacement. Beside some minor deviations that are visible within the measured results of Fig. 6.17(c), it is shown that the characteristic is unchanged for different and even asymmetric supplies within an absolute minimum and maximum range of 3.3 V and 38 V respectively. Different than expected from simulation [83], increasing the supply voltage beyond 38 V decreases the performance slowly. The problem was inferred to a leakage current that increases to more than 20 nA in two additional HV measuring pads, connected to $V_{\mathrm{HV+}}$ and $V_{\mathrm{HV\text{-}}}$. However, a very high supply voltage of 38 V does still outperform consequence-based state-of-the-art active charge balancers.

The system was also tested in an in-vitro environment with platinum electrodes in phosphate-buffered saline solution. By applying the method of [87], the parameters of the provided electrode were found to be around $C_{\mathrm{H}} \approx 1.1\,\mu\mathrm{F}$, $R_{\mathrm{F}} \approx 75\,\mathrm{k}\Omega$ and $R_{\mathrm{S}} \approx 2.1\,\mathrm{k}\Omega$. The stimulator front-end, as described in sec. 4.3, was used to apply stimulation pulses with a pulse width of 3.5 ms and an intended mismatch between cathodic and anodic stimulus. First, in Fig. 6.18(a), an unbalanced biphasic pulse with cathodic amplitude of around 700 µA and an anodic one of around 1.2 mA, caused a remaining voltage V_{E} of 1.6 V with respect to V_{CM}. This voltage is clearly larger than the defined safety limit of ±100 mV, resulting in negative compensation currents I_{IPCC}. Depending on the setting of the maximum I_{IPCC} limit, the peak compensation current amplitudes and compensation times differ from each other. For all three maximum I_{IPCC} settings, V_{E} decreases gradually and reaches the safety limit within a compensation time that is less than the time of repetition of the stimulation. Second, in Fig. 6.18(b), a monophasic cathodic stimulus of around 700 µA in amplitude was applied. A large remaining V_{E} of around −2 V activates the maximum I_{IPCC}, according to the settings. The larger the compensation current limit is, the faster V_{E} approaches the safety limit. The example of monophasic stimulation shows, that the IPCC system is able to compensate a mismatch of up to ±100% with respect to the safety limit. Thus, the missing anodic counter pulse is autonomously replaced, which makes the charge balancer suitable for stand-alone applications, e.g. as a complement to monophasic stimulators. In Fig. 6.18(a) the biphasic stimulus has a symmetric supply of ±10 V, whereas in (b) a monophasic

stimulus with an asymmetric supply of +3.3 V and -10 V was chosen. Thus, the measured results of Fig. 6.18 verify the same CB efficacy at different supplies, since the differential output voltages $V_{\mathrm{LV+}}$ and $V_{\mathrm{LV\text{-}}}$, as well as $V_{\mathrm{HV+}}$ and $V_{\mathrm{HV\text{-}}}$, stay within their $\triangle \mathrm{V_{LV}}$ domains of 3.3 V.

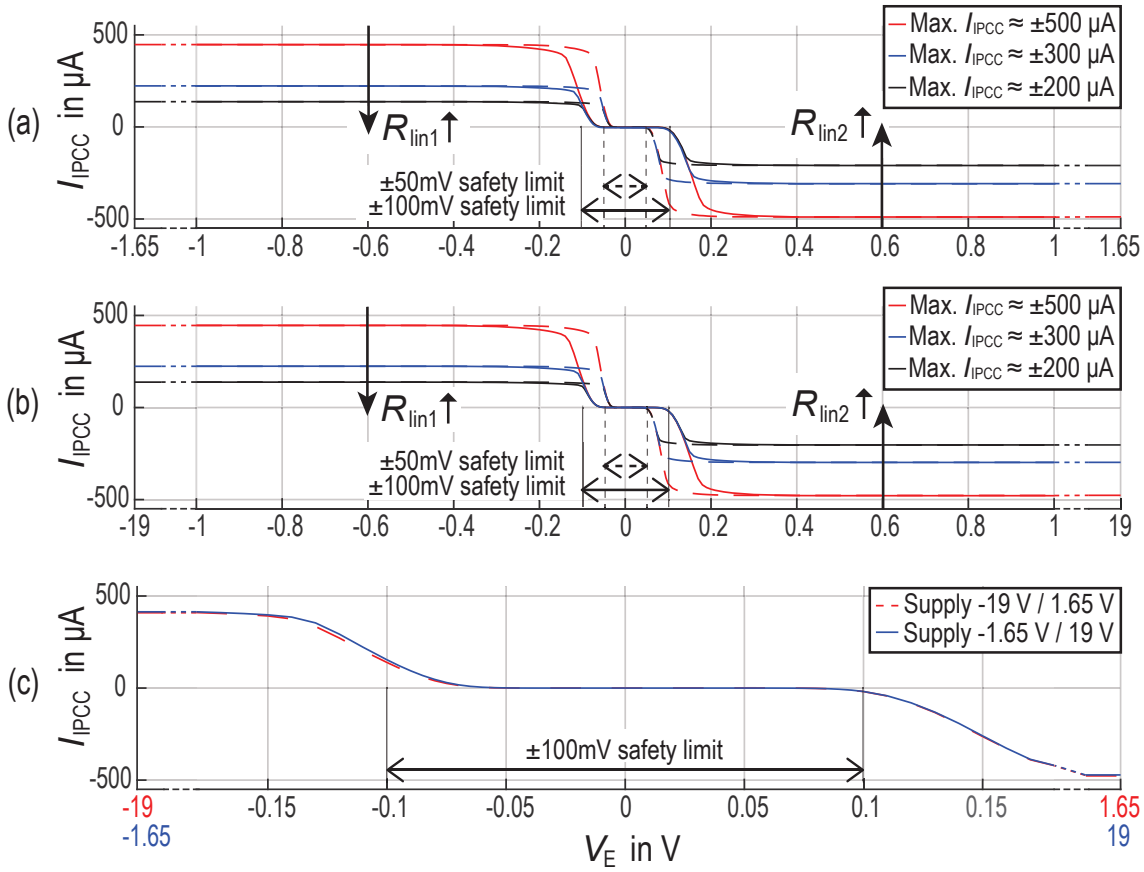


Figure 6.17.: Measured results of the compensation current I_{IPCC} versus V_{E} prove that the characteristic is unchanged for (a) a min. supply of ±1.65 V, (b) a max. supply of ±19 V, and (c) an asymmetric supply of +19 V/-1.65 V and -19 V/+1.65 V, with respect to V_{CM}. In (a) and (b) the results of all three $R_{\mathrm{lin1,2}}$ settings are shown. Additionally, the solid lines correspond to a safety limit setting of ±100 mV, the dashed ones to ±50 mV. In the zoomed view of (c) I_{IPCC} is exemplarily shown with min. $R_{\mathrm{lin1,2}}$ setting and ±100 mV safety limit, to visualize the displacement of the actual dead-zone from the safety limit [86] (©2021, IEEE).

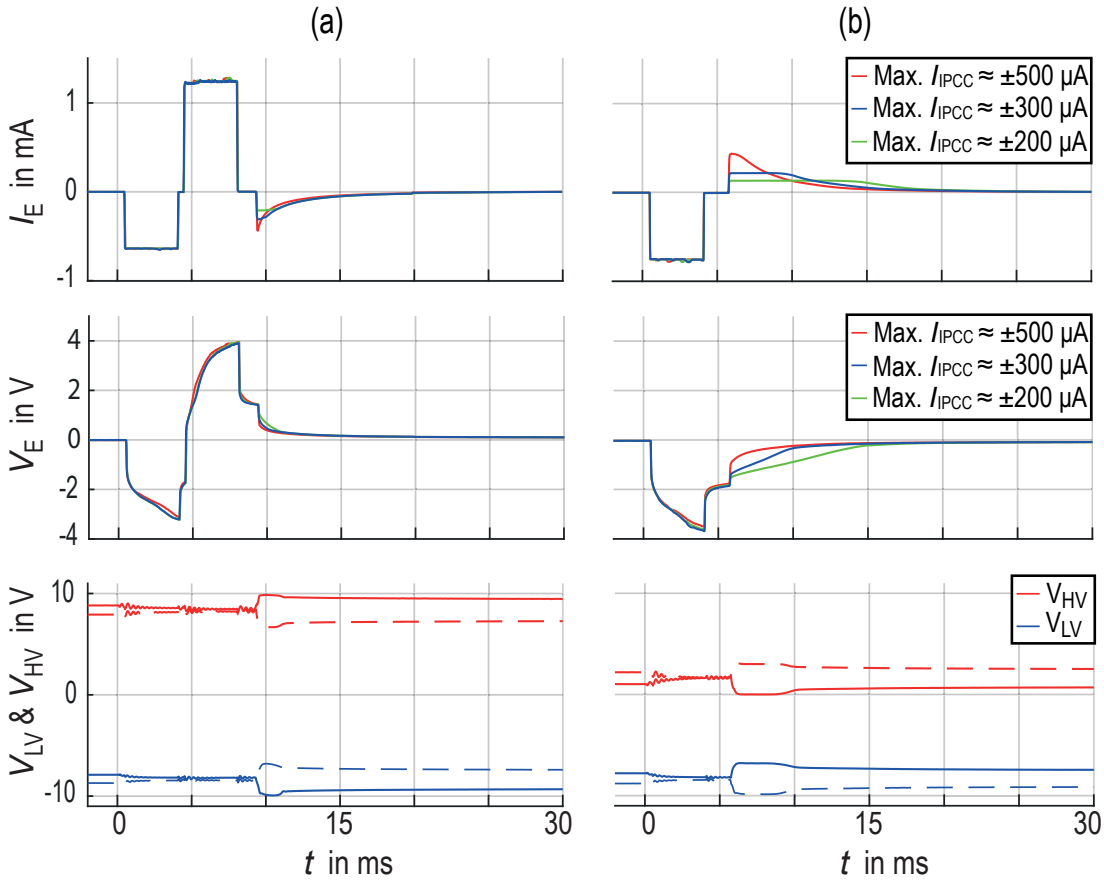


Figure 6.18.: Measured in-vitro charge balancing results for a platinum electrode in saline solution and a safety limit of ±100 mV with (a) a symmetric supply of ±10 V, and (b) an asymmetric supply of +3.3 V and -10 V [86] (©2021, IEEE).

6.4. Stability Considerations

Both IPCC implementations represent feedback control loops that can be converted into the standard control representation, shown in Fig. 6.19. The control consists the monitoring amplifier as the P controller $P(s)$ of constant gain and output voltage V_G that steers a subsequent current driver. The latter introduces another gain stage $G_m(s)$ whose gain is dependent on the actual working point. The system is defined by the electrode-tissue interface $Z_E(s)$. Via a direct feedback path, V_E is subtracted from the target value, which is the body's quiescent potential V_{CM}. In case of an initial mismatch current or disturbance, for example in form of a cross coupling current, the electrode voltage becomes

$$V_E(s) = \frac{A(s) \cdot V_{CM}}{1 + A(s)} + \frac{Z_E(s) \cdot I_{mismatch}}{1 + A(s)} , \tag{6.15}$$

with the loop gain

$$A(s) = P(s) \cdot G_m(s) \cdot Z_E(s) . \tag{6.16}$$

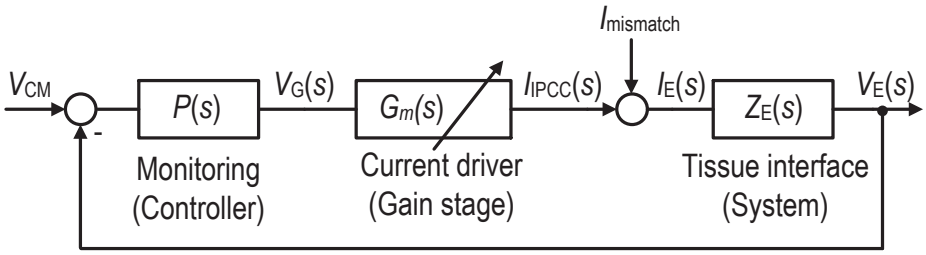


Figure 6.19.: The IPCC in its standard feedback control loop representation [86] (©2021, IEEE).

The current driver provides an additional feature of inherent hysteresis for safety window detection that introduces a dead-zone around the target value. The continuous operation with decreasing compensation amplitude for decreasing remaining V_E provides a smooth transition into the safety window, making overshoots impossible, and thus, providing inherent stability. In contrast to the short pulse insertion [4], this is an advantage since the stability is not dependent on individual and discrete charge packages. Large packages might cause the electrode voltage to step over or step under the safety window and result in a ringing steady state potential [9].

The stability during operation of both IPCC circuits was examined for different operating points to cover the dynamic working range. Thus, outside the dead-zone, the phase margin of the IPCC-22 V compliance was found to lie between 95° to 126°, simulated at C_H of 0.1 µF, R_S of 1 kΩ and R_F of 1 MΩ. The stability analysis of the closed loop system has been performed at several working points and settings and the system was found stable. The phase margin of the IPCC-AS mainly lies at a similar but slightly lower range. For an exemplary stimulation with safety limit of ±50 mV, the phase margin at a remaining electrode voltage of +70 mV is around 72.5° at a unity gain frequency of 160 kHz. At a remaining electrode voltage of -70 mV the phase margin is around 85.25° at a unity gain frequency of 190 kHz. Moreover, during the transient analysis of various scenarios, no oscillations of the compensation currents were observed. Both IPCC systems showed a stable behavior.

6.5. Comparison to State-of-the-Art Consequence-Based Systems

Consequence-based charge balancing systems of previously published stimulators use passive charge balancing or active charge balancing by short pulse insertion. The Inter-Pulse Charge Control represents a novel stand-alone method for consequence-based active CB. The most significant advantage of the IPCC compared to passive charge balancing is the ability to control the compensation current intensities. Additionally, all remaining charges that were supplied externally will be actively

compensated, and not only by a redistribution within the tissue, which might lead to cross-talk. Compared to the short pulse insertion methods [4, 6, 34, 48], IPCC provides continuous charge compensation with decreasing amplitude, inherent stability and avoids digital activity at the tissue interface. By inherently incorporating hysteresis because of its class-B architecture, the IPCC offers a self-regulated and reference-free removal of charges. With an overall simple design it showes advantages in terms of effectiveness, where in contrast to e.g. [4, 6, 34, 48] additional voltage references or control units to define and detect the safety window are dispensable.

A comparison between the improved IPCC-AS and its predecessor IPCC-22 V with state-of-the-art active consequence-based balancers is presented in Tab. 6.5. The presented IPCC designs (IPCC-22 V and IPCC-AS) feature HV robustness, IPCC-22 V with a fixed 22 V supply. The improved IPCC-AS, however, offers high adaptability in terms of supply voltage compliance from 3.3 V to 38 V. Further, the system efficacy of IPCC-AS is unchanged at asymmetrically arranged supply rails with respect to the body's quiescent potential V_{CM}. The maximum voltage compliance of 38 V is the highest compared to the state-of-the-art. Both IPCC balancers are very power-efficient. In the stationary state, IPCC-22 V consumes 37.1 µW only. The power consumption of the IPCC-AS circuit (pads excluded) is as low as 6.3 µW at a 3.3 V supply. Even at a HV supply of 38 V the power consumption is 24.6 µW, which is only a fraction of the power dissipation of the HV comparator employed in [4, 34].

The charge balancing implementation of [48] consumes more than seven times the power of the IPCC at the same supply voltage. The implemented HV comparator in [4] is referred to the one of [34], concluding a consumption of 438 µW. As mentioned before, the power consumption of 0.4 µW that is stated in [4], must be reached by a duty cycle with very short activation time of the HV comparator within one stimulation interval. However, the activation time is not given in [4] and will differ from one interval to another, since the short pulse insertion method requires an unknown amount of compensation pulses, dependent on the amount of mismatch. The charge balancing implementation of [48] consumes more than seven times the power of this work at the same supply voltage. Only [88] has a power dissipation comparable to the work presented in this paper.

The die area of around 0.2 mm^2 still needs to be improved. It is much larger compared to the short pulse insertion of [4, 34], but comparable to other charge balancers like [48], as well as [28] and [31] that use 0.33 mm^2 and 0.16 mm^2 respectively. For IPCC-22 V and IPCC-AS additional flexibility is given by two configurable safety limits of ±50 mV or ±100 mV, as well as three configurable maximum compensation current amplitudes, adjustable between ±150 µA and ±500 µA. As long as V_{E} stays within the predefined safety window the current driver of the IPCC system becomes automatically inactive and consumes no power. The IPCC is the only known approach with self-adaptive timing. The simple design methodology and its configurable charge balancing characteristics offer good adaptability to various neural stimulators.

Table 6.5.: Comparison of state-of-the-art consequence-based active charge balancers.

Reference	JSSC 2007 [34]	JSSC 2012 [4]	JSSC 2013 [6]	ASSCC 2015 [48]	ISCAS 2019 [88]	**This work** IPCC-22 V	IPCC-AS
Consequence-based CB methods	Preprogrammed short pulse insertion	Preprogrammed short pulse insertion	Preprogrammed short pulse insertion	Pulse width adaption with pulse insertion	Synchronous charge balancing	Autonomous IPCC & counter pulse generation	Autonomous IPCC & counter pulse generation
Process	0.35 µm	0.35 µm	0.5 µm	0.18 µm	0.18 µm	0.35 µm	0.35 µm
Max. voltage compliance	22.5 V	20 V	4.6 V	20 V	10 V	22 V	3.3 V to 38 V
Power consumption	468 µW of HV comparator	0.4 µW (438 µW ***)	N/A	110 µW	6.4 µW	37.1 µW	6.3 µW to 24.6 µW
Die area	0.03 mm^2 *	0.03 mm^2 ***	N/A	0.105 mm^2	0.086 mm^2	0.261 mm^2	0.208 mm^2
Safety window detection	±50 mV by HV window comparator	±100 mV by HV window comparator	±50 mV by on-chip controller	Detection of pulse polarity by VMQQ****	<20 mV comparator	±50 mV or ±100 mV by intrinsic idle window	±50 mV or ±100 mV by intrinsic idle window
CB currents	±250 µA**	±100 µA*	±20 µA	±78 µA	< ±30 µA	≤ ±500 µA	≤ ±500 µA
CB duration	5 µs per spike	25 µs per spike	20 µs per spike	5 µs per spike	50 µs**	Self-adaptive	Self-adaptive

$^{(*)}$estimated

$^{(**)}$same as stimulus

$^{(***)}$estimated from [34], because [4] refers to the HV comparator of [34]

$^{(****)}V_{\mathrm{res}}$ monitoring and Q_{res} quantization circuit

6.6. Summary

According to the consequence-based compensation technique, the Inter-Pulse Charge Control eliminates excess charges instantaneously, and reduces V_{E} towards the safety limits after each stimulus. The presented IPCC concept is novel and consists of a monitoring amplifier and a class-B stage as the compensation current source. Two design versions are implemented in this work. Both IPCC circuits feature HV robustness. However, IPCC-22 V is fixed to a 22 V supply, where as the compensation current of the improved IPCC-AS is independent of the supply voltage within the range of 3.3 V to 38 V. Further, the system efficacy is unchanged at asymmetrically arranged supply rails with respect to the body's quiescent potential V_{CM}. Although providing HV robustness, both balancers are power-efficient, and consume between 6.3 µW to 37.1 µW only. Additional flexibility is given by two adjustable safety limits, ±50 mV or ±100 mV, and by three configurable maximum compensation current amplitudes up to ±500 µA. Two different methods for limiting the maximum output current were compared, either decreasing the dynamic range by an earlier pinch off via R_{lin} or flattening the output slope of I_{IPCC} by source degeneration via R_{sd}. Both IPCC implementations represent feedback control loops with a P controller of changing gain for different working points. However, the intrinsic hysteresis of the class-B stage, used for safety window detection, features inherent stability. Due to the autonomous and flexible charge balancing characteristics and its ability of generating a complete counter pulse by an amplitude-controlled continuous current supply, the IPCC is not only suitable as stand-alone charge balancer for arbitrary neural stimulators, but also as a complement to monophasic stimulators.

7. Twin-Track Charge Balancer

In addition to a separate usage of the PI-controlled Offset Compensation (chapter 5) and the IPCC (chapter 6), both active charge balancers can be combined together to improve the performance. Their conjunction is termed Twin-Track[11] charge balancer, since it combines the cause-based and consequence-based CB techniques. With the Twin-Track system it is possible to choose the appropriate charge balancing method for a target application. The PI-controlled OC reaches a stable charge balanced state by counteracting the cause of the emergence of charge mismatch, and therefore, is important for long-term trials with chronic implantation. However, OC methods usually show a settling process with overshoots during startup. Therefore, in short-term trials with seldom stimulation triggering, these methods are not appropriate and the consequence-based method of the IPCC is preferred. Also for long-term stimulation applications with higher charge mismatch within the stimulation source, offset regulation alone cannot initially compensate the mismatch. The overshoots can be reduced or even eliminated by combining the OC with short-term charge balancing methods like the IPCC, in which remaining charges are compensated directly after each unbalanced biphasic stimulation pulse. In the following, the Twin-Track system setup is described and measurement results[12] are presented.

7.1. Twin-Track System Setup

This section presents the combined cause-based and consequence-based Twin-Track charge balancing system, illustrated in Fig. 7.1. Both charge balancing controls are based on the monitoring of V_{E}, which automatically incorporates any mismatch, self-discharge or other disturbances at the electrode-electrolyte tissue interface. Therefore, the node of V_{E} is the connection node of the individual controls. The PI-controlled OC (chapter 5) is the cause-based CB system. The consequence-based CB system is the IPCC-22 V (sec. 6.2), that is restricted to a fixed supply. Since the same voltage supply is taken for the complete system, including both balancers and the stimulator, the overall $V_{\mathrm{DD\_HV}}$ is fixed to 22 V. The Twin-Track balancer consumes 56 µW at 22 V [13]. A conjunction of the PI-controlled OC with the IPCC-AS (sec. 6.3) instead, will improve the Twin-Track system in terms of flexibility and

[11] The idea of a combination of two complementary active charge balancing methods to a CMOS integrated 'Twin-Track' system emerged from the preliminary work [15] of the author of this thesis.

[12] The measurement results of the Twin-Track system have been published in [13, 63] (©IEEE).

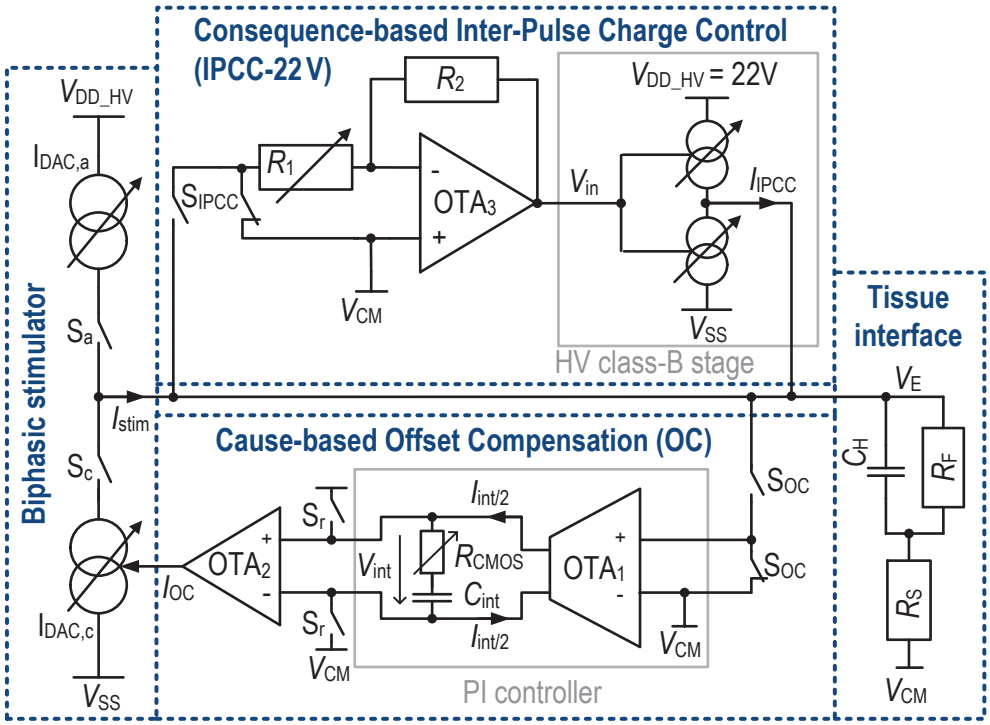


Figure 7.1.: Concept of the cause-based and consequence-based Twin-Track active charge balancer. Modified from [13] (©2018, IEEE).

adaptability of the supply voltage. However, at the time of these measurements, the IPCC-AS was still under investigation. Anyway, according to the results of the system validation in sec. 6.3.5 the efficacy is expected to be equivalent.

The PI-controlled OC and the IPCC were joined to the Twin-Track system on PCB level as shown in Fig. 7.2. Chip 1 consists of the biphasic current-controlled stimulator and the PI-controlled OC circuit with 1.23 mm^2 and 0.45 mm^2 of die area, respectively; Chip 2 contains the IPCC-22 V with 0.26 mm^2. The switches S_{IPCC}, S_{OC} and S_r are controlled by a FPGA (sec. A.2) with respect to the stimulation pulses. Both charge balancers can be activated independently via S_{IPCC} and S_{OC}, either alone for a single usage, or subsequently for a Twin-Track run according to the signal flow diagram shown in Fig. 7.3. The initial state of S_{OC} and S_{IPCC} is 'open', ensuring that during stimulation both charge balancers stay inactive. If needed and at the beginning of a new stimulation trial, the OC can be reset by discharging C_{int} via S_r. Directly after each stimulus, S_{OC} is high for an interval of 300 µs to measure V_E, the corresponding mismatch value is stored on C_{int}. Subsequently, S_{IPCC} turns high and the IPCC starts monitoring V_E, balancing the remaining charges instantaneously. S_{IPCC} stays high until the next stimulus starts, thus being able to react to disturbances. However, the current supply of the IPCC becomes inactive autonomously, usually before the next stimulus, once V_E has reached the safety limits.

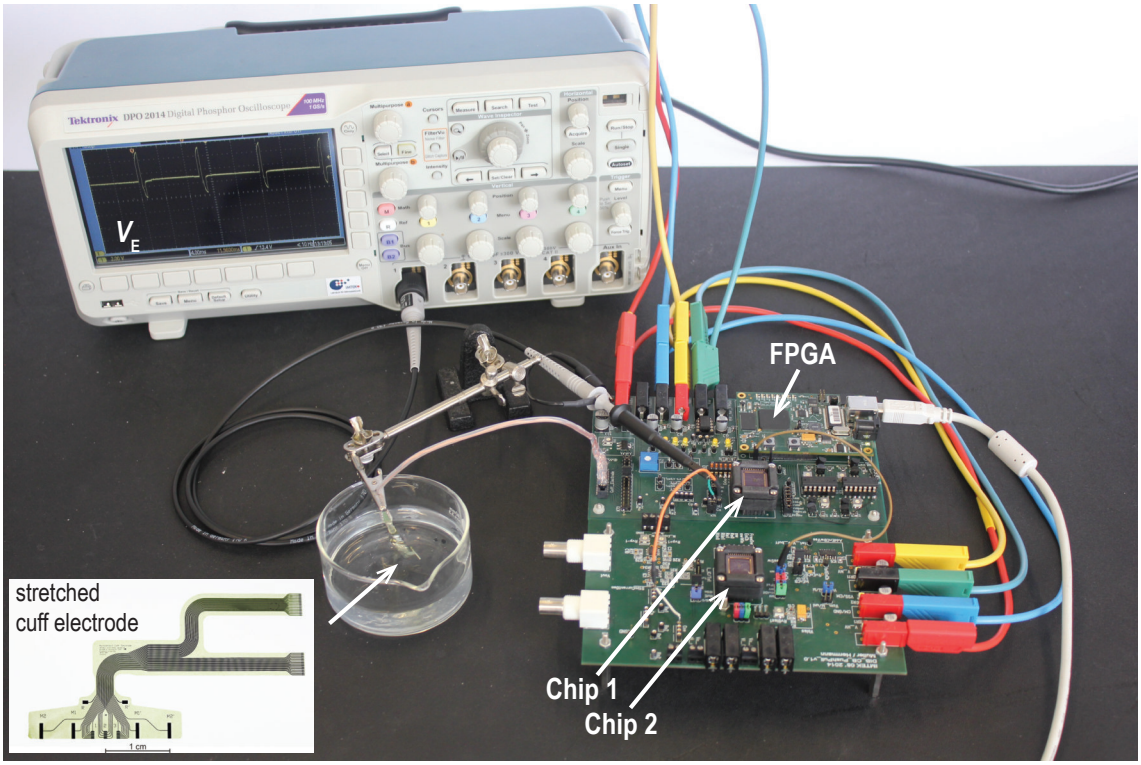


Figure 7.2.: Running in-vitro measurement setup showing the polyimide thin film cuff electrode in 0.9% saline solution and the PCB containing the two chips and the FPGA that provides the digital control signals. [13] (©2018, IEEE).

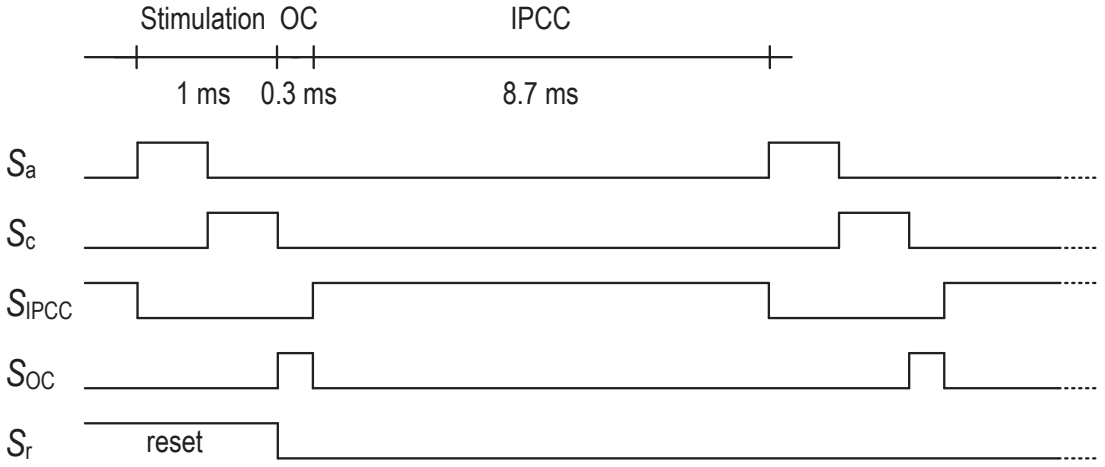


Figure 7.3.: Signal flow diagram, illustrating the timing of the Twin-Track active charge balancing system. Modified from [13] (©2018, IEEE).

7.2. Twin-Track Measurement Results

To measure the Twin-Track system behavior, an intentional mismatch in cathodic and anodic stimuli was generated. Therefore, the on-chip stimulator prototype, capable of generating amplitudes from 1 µA to 5.12 mA with 9-bit resolution, was controlled by the external FPGA. The system was measured with an electrode equivalent model as well as in an in-vitro environment.

7.2.1. System Measurements

The charge balancing characterization of the Twin-Track system was validated by an electrode equivalent model with R_S of 1 kΩ, R_F of 500 kΩ and C_H of 0.1 µF, which is the smallest expected capacitance of the given cuff electrode, thus, providing the largest effect on charge balancing. The impact of the PI-controlled OC, the IPCC, and their Twin-Track combination, compensating a mismatch of 36% is presented in Fig. 7.4. During the first stimulus, shown in zoom 1 of Fig. 7.4(a), the PI-controlled OC alone does not yet have a charge balancing effect, and therefore, V_E exhibits an offset voltage. However, after some pulses the system settles and V_E is kept at V_{CM}, reaching a long-term stable state by cathodic amplitude correction, as shown in Fig. 7.4(a) zoom 2 at 0.5 s. While the offset compensation method demands an initial settling, the IPCC (Fig. 7.4(b)) compensates remaining charges instantaneously from the first pulse on. Since the IPCC does not counteract the origin of the mismatch, it exhibits repeated activation over time. Consequently, the compensation response in the second zoom is similar to the response of the first stimulus. When using both systems simultaneously, as a Twin-Track balancer (Fig. 7.4(c)), highest efficacy in terms of a charge balanced V_E is achieved. By means of the IPCC an instantaneous charge compensation right from the first pulse on can be guaranteed, and additionally, a long-term stable state is reached by PI-controlled OC, equalizing the stimulation charges. Thereby, the IPCC is active only during the settling of the OC with decreasing compensation intensities. After settling, the OC reduces the need for additional pulses between stimulations, increasing the efficacy of the system. As beneficial fail-safety backup, the IPCC would furthermore activate itself in case of unforeseen disturbances in form of V_E voltage spikes, e.g. due to a crossover of nearby stimulations, or in case of malfunction of the stimulation sources.

7.2.2. In-Vitro Measurements

The Twin-Track active charge balancer was tested in an in-vitro environment with a polyimide thin film cuff electrode [8] in 0.9% saline solution, illustrated in Fig. 7.2. A stimulation pulse of 1 mA with 30% mismatch was applied. The parameters for the provided electrode were found to be around C_H of 1.3 µF, R_F of 100 kΩ and R_S of 3 kΩ by applying the method of [87]. In Fig. 7.5(a) the imbalanced stimulation

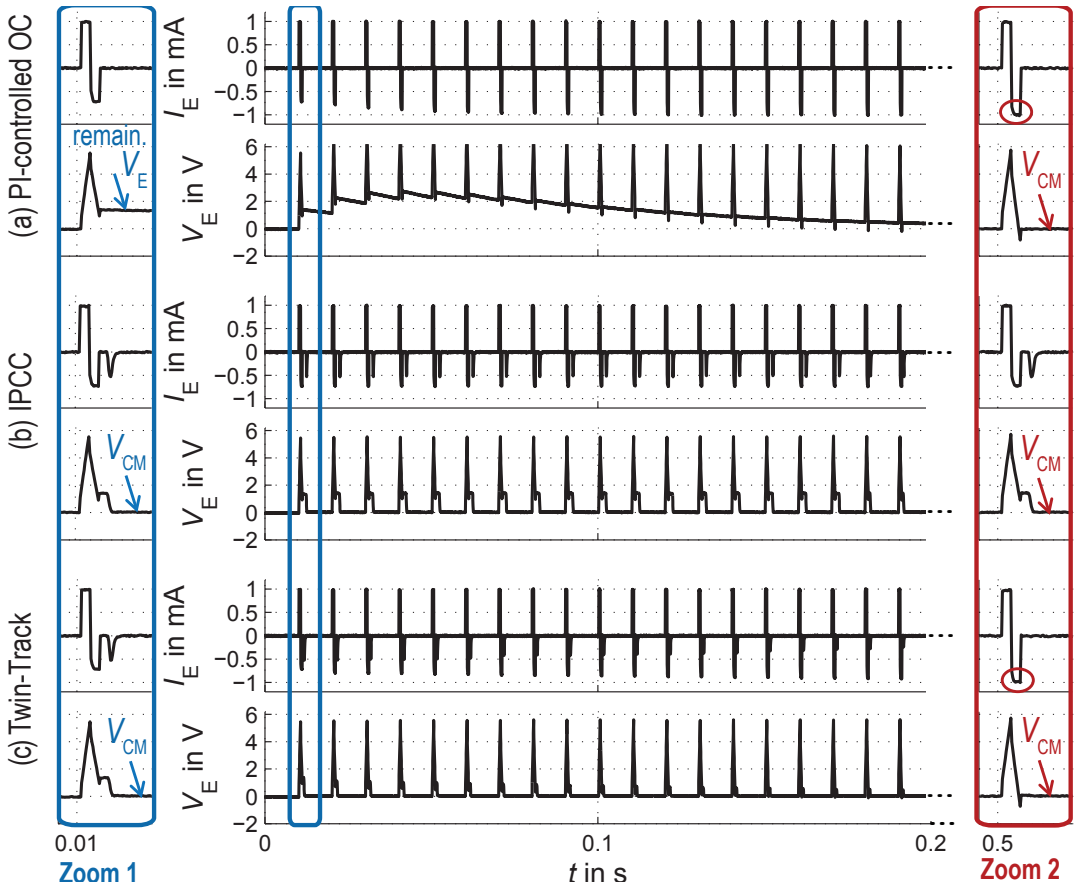


Figure 7.4.: Twin-Track measurement results for a biphasic stimulation pulse with intended mismatch of 36%, showing the control behavior of (a) the PI-controlled OC, (b) the IPCC, and (c) their Twin-Track combination. [13] (©2018, IEEE).

condition (no CB) of V_E is compared to the charge compensation process of (a) the PI-controlled OC, (b) the IPCC, and (c) their Twin-Track combination. It is clearly visible that in (a) without CB, the introduced mismatch will lead to a harmful permanent electrode potential of around 1.2 V. However, in (b-d) using PI-controlled OC, IPCC or their combination, V_E is successfully kept within the safety window. The operation of the PI-controlled OC and the IPCC are barely visible within the representation of Fig. 7.5(a) and (b). Therefore, the comparison of the PI-controlled OC and the IPCC is added in Fig. 7.6. The rather large capacitance C_H causes a slow rise of the resting potential. Thus, the integration steps on C_{int} are relatively small and result in a slow settling of the PI-controlled OC, despite a well adjusted value of R_{CMOS}. However, a long-term stable state is reached and the stimulation charges are equalized after around 1.5 s. Considering IPCC, compensation currents of around 40 µA were sufficient to reduce V_E into the safety window. The in-vitro results in Fig. 7.6(b) show that the I_{IPCC} is not exploited to its maximum current limit for successful balancing. The measured I_{IPCC} compensation current yields 0.04% of the stimulation current only, thus not risking an unwanted restimulation of the nerve.

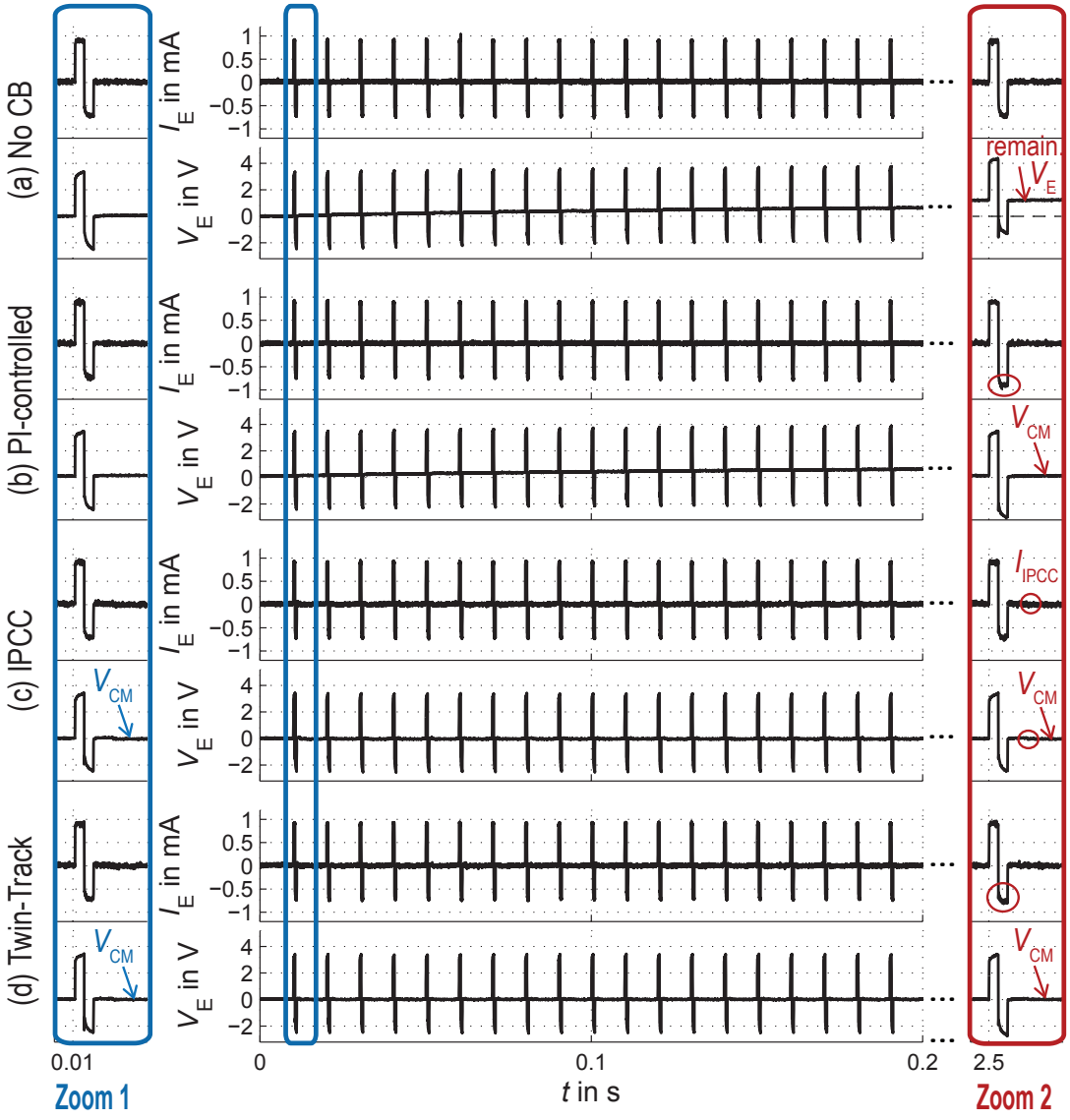


Figure 7.5.: In-vitro results measured with a polyimide thin film cuff electrode in 0.9% saline solution, for a biphasic stimulation pulse of 1 mA and 30% mismatch. In (a) the emergence of a remaining electrode voltage due to the absence of CB is shown. In (b) the efficacy of the PI-controlled OC, in (c) of the IPCC, and in (d) of their Twin-Track combination is shown.

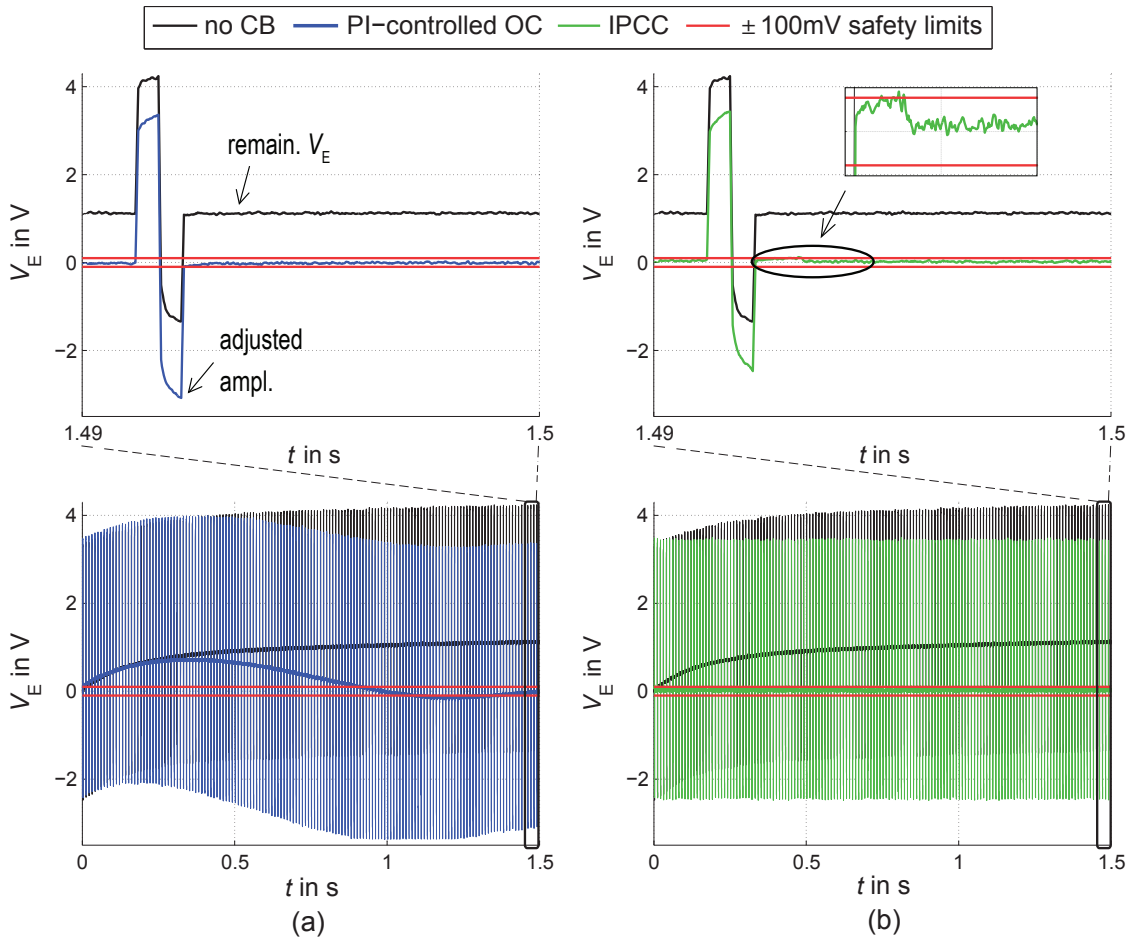


Figure 7.6.: The imbalanced stimulation condition (no CB) is compared in (a) to the settling behavior of the PI-controlled OC, and in (b) to the IPCC's immediate and continuous charge compensation after each stimulus. The settled condition is illustrated for each graph by a zoomed view. [13] (©2018, IEEE).

7.3. Summary

The combination of cause-based and consequence-based charge balancing techniques to a Twin-Tack balancer promises a big success, since it takes benefit of the advantages of both techniques. The two charge balancing systems are activated subsequently, so that the PI-controlled OC shortly monitors and stores the information about the remaining electrode voltage, before the IPCC compensates the residual charges. In this way, the charge compensation is guaranteed after each stimulation pulse and at the same time, long-term charge equalization is achieved in the background by counteracting the cause of the charge mismatch.

8. Conclusion and Outlook

8.1. Conclusion

Modern implantable neural stimulators have become highly specialized and adjustable to the challenges of diverse applications. Within this work a highly adaptive and power-efficient current-controlled stimulator front-end is presented, consuming 20.8 µW at 3.3 V supply. The achieved compliance range of 3.3 V to 49 V is outstanding compared to state-of-the-art. The stimulator features arbitrary waveform generation with current amplitudes from ±2 µA to ±10 mA and 8-bit resolution per DAC. Despite multiple setting options mismatch in a current waveform may always occur due to process variations in integrated circuits. Therefore, active charge balancing as an important safety aspect of neural stimulators is indispensable. The presented stimulator front-end is compatible with the developed active charge balancing methods and is used for all system and in-vitro measurements. Due to the high voltage stimulation environment, all interface components and circuits must be HV compliant. Therefore, the circuit design is based on a quad-rail methodology and components like a HV compatible switch and HV level translator were developed.

In this thesis, the main focus lay on the design and implementation of the CMOS integrated active charge balancing circuits. Two charge balancing concepts were elaborated, based on the monitoring of the electrode voltage, which automatically incorporates any mismatch, self-discharge or other disturbances at the electrode-electrolyte interface. The cause-based system is named PI-controlled Offset Compensation (OC), since it corrects the negative stimulus amplitude in the background to reach a stable charge compensated state. The maximum voltage compliance of this work is 30 V, which is the highest reported compared with other integrated charge balancing circuits. Despite the HV implementation, the power dissipation is very low. The system consumes 18.9 µW measured at an exemplary HV supply of 22 V. However, the die area dissipation of this analog OC implementation has area disadvantages compared to digital OC solutions and needs to be improved. The balancer's monitoring amplifier design provides an extraordinary small transconductance of 1.5 nS, and thus, achieves a large time constant of 8 ms with only a 12 pF on-chip capacitor, which leads to the first integrated PI-controller for offset compensation in neural implants. In conjunction with the stimulator front-end, the PI-controlled OC is capable of up to ±36% biphasic stimuli mismatch correction. The compensation precision with respect to the body's quiescent potential is

±20 mV. Simulation and measurement results proved that a PI-control is beneficial compared to an I- or PT-control. It's transfer function provides an additional zero, adding a further degree of freedom for stability adjustments to adapt to a wide variety of electrodes.

The Inter-Pulse Charge Control (IPCC) represents a novel stand-alone method for consequence-based active CB. It provides self-regulated charge compensation after each stimulus by a continuous but amplitude-controlled compensation current with decreasing intensity. The novelty of this approach is to make use of the inherently incorporated hysteresis of the implemented class-B architecture. The main advantage of the presented IPCC is its instantaneous effectiveness with an overall simple design, where in contrast to state-of-the-art solutions additional voltage references are dispensable. Additionally, it provides inherent stability and avoids digital activity at the tissue interface. Two IPCC circuits (IPCC-22 V and IPCC-AS) were implemented. Both IPCC implementations feature HV compliance. In contrast to the IPCC-22 V circuit that is limited to a fixed 22 V supply, the IPCC-AS circuit overcomes these technology limitations by its design using the configurable quad-rail architecture. The maximum achieved voltage compliance of 38 V is the highest reported for consequence-based active charge balancers. Additionally, it was shown for IPCC-AS that the compensation current is independent of the supply voltage within the range of 3.3 V to 38 V. Further, the system efficacy is unchanged at asymmetrically arranged supply rails with respect to the body's quiescent potential V_{CM}. For both implementations, additional flexibility is given by safety limits configurable to ±50 mV or ±100 mV, as well as three configurable maximum compensation current amplitudes, adjustable between ±150 µA and ±500 µA. Both IPCC implementations are very power-efficient. As long as V_{E} stays within the predefined safety window the current driver of the IPCC systems becomes automatically inactive and consumes no power, thus, providing a self-adaptive timing. In the stationary state, the measured power consumption of the IPCC-22 V is 37.1 µW only. The power of the IPCC-AS is as low as 6.3 µW at a 3.3 V supply. Even at a HV supply of 38 V the power consumption is 24.6 µW only. The various configurable CB characteristics offer good adaptability to various neural stimulators. The provided user friendly stand-alone functions, have the merit of complementing already certified stimulation systems, and reducing the programming and circuit overhead, since it works autonomously and independent of the stimulator unit.

The combination of the PI-controlled OC and the IPCC to the Twin-Track system represents a CMOS integrated active charge balancer, accomplishing cause-based and consequence-based compensation. Thus, the Twin-Track system consists of a close loop balancer for an analog background operation as well as a self-adaptive balancer for automatic counter pulse generation. This is especially advantageous for achieving long-term stability with instantaneous tissue protection. All circuits were manufactured in a 0.35 µm HV CMOS process and verified by chip and in-vitro measurements.

8.2. Outlook

Phase margin $I_{DAC,a}$: The PM of the $I_{DAC,a}$ of the stimulator is rather small and further optimization is recommanded in sec. 4.3.2. One suggestion is to push the transfer function towards a one pole system by splitting the two dominant poles, but further investigations are needed.

Die area: The presented CB circuits were not optimized for size yet, instead the focus lies on the flexibility for arbitrary use and functionality. However, there is still potential to minimize the area of the CB systems of this work when specialized for a certain application. The presented IPCC is comparable in size to the charge monitoring system presented in [27, 28, 31] and pulse width adaption of [48], but much larger than the charge balancer of [4]. The IPCC provides different options to limit the maximum allowed compensation current. However, each setting requires a HV logic level shifter as illustrated in Fig. 6.4. Additionally, the presented design allows configuring the safety window. Realizing the IPCC as an application specific design with preset safety limits and predefined compensation limits, allows a reduction of the overall area by around 42%.

The area of the presented OC realization is around 36% of the area of the stimulator front-end itself before any area optimization. The main area contribution of the OC system comes from the input transistors of OTA_1. Designing the input stage of OTA_1 for a smaller dynamic input range requirement than the assumed 6 V, reduces its active area significantly. As an example, reducing the input range of OTA_1 by only a factor of $\sqrt{2}$, reduces the area shown in no. 1 of Fig. 5.13 by a factor of 2. An analog response of the system (instead of quantized step sizes) is guaranteed as long as the differential input voltage stays within the input range of OTA_1. Thus, the input range requirement can be reduced and the analog integration behavior of the PI-controller is still preserved, if smaller stimulation amplitudes, mismatch, pulse widths, or Helmholtz capacitance C_H are expected, than assumed in the worst case scenario of (5.17). Further area reduction, leading to an operation outside the dynamic input range, is also possible without hindering the functionality of the system, but would result in quantized integration steps until V_E is decreased to a value within the input range. Additionally, for LV stimulator applications up to 5 V, it is recommendable to redesign the input stage using LV transistors only. A wide input range demands for a small W/L ratio. However, the HV transistors of the employed technology are inherently wide. Compared to the LV transistors, the minimum width of the HV transistors is 12-times larger, resulting in a die area multiplied by 144 for the same W/L ratio. Another possibility to reduce the die area is by minimizing the configurability of the R_{CMOS} values of the PI-controlled OC. The area of no. 3 in Fig. 5.13 is linearly dependent on the configuration possibilities. It is shown in Fig. 5.12 that the system is stable for changes in electrode values like expected for example due to tissue growth. Therefore, for an application specific usage, where the electrode parameters are roughly known, a reduction of the configuration possibilities from 5 to 2 bits will decrease the area by 87.5%.

Power consumption: The power consumption of each circuit was kept very low despite the HV supply. However, the current flows continuously so far. State-of-the-art solutions disconnect the charge balancers during stimulation intervals to save power. In this way, [4] reaches an exceptionally low power consumption of 0.4 µW per duty cycle. The OTA_1 of the PI-controlled OC circuit is only active for around 300 µs. The inherent hold characteristic of C_{int} makes it possible to put a disconnection from the supplies into practice, as long as the OTA_1 does not need to be active. As a comparable example, the power consumption of the OTA_1 of the PI-controlled OC for the duty cycle of 10 ms at a 20 V supply would result to

$$P_{\text{IPCC}} = (610\,\text{nA} \cdot 20\,\text{V} + 300\,\text{nA} \cdot 3.3\,\text{V}) \cdot \frac{300\,\mu\text{s}}{10\,\text{ms}} = 0.4\,\mu\text{W}\,. \tag{8.1}$$

Adding the continuous power of OTA_2 and the HV switches (see Tab. 5.2) results in an overall OC power consumption of around 2 µW instead of 15 µW per duty cycle.

The activation time of the IPCC can be reduced by the time of the stimulus itself, which reduces the power consumption by 10%. An even more significant power reduction could be realized by stopping the activation once V_{E} is reduced within the safety range. However, the intention of the autonomous and stand-alone IPCC was to have a continuous monitoring in between the stimulation phases, to intervene in case of any disturbances. Thus, as beneficial fail-safety backup, the IPCC activates itself in case of unforeseen voltage spikes, e.g. after nearby stimulation, or in case of malfunction of the stimulation source.

Voltage compliance PI-controlled OC: The maximum voltage compliance of the PI-controlled OC is 30 V, restricted by the V_{GB} operating condition of the employed HV technology. However, this restriction can be avoided by connecting the bulk terminals of the input transistors to the source terminals instead of $V_{\text{DD\_HV}}$. Thus, the voltage compliance can be increased to 48 V.

Twin-Track measurements: The measured Twin-Track results relay on the conjunction of the PI-controlled OC with the IPCC-22 V. However, the Twin-Track system would be improved in terms of flexibility and adaptability of the supply voltage if the IPCC-AS is used. Even though the results are expected to be equivalent, validation is still required.

In-vitro investigations: The presented stimulator including charge balancing provides great flexibility for arbitrary use. The functionality has been tested in an in-vitro environment. The next step is to go to in-vivo trials. The stimulator suggests itself for investigations involving the efficacy of different current waveform shapes. Considering charge balancing, results from in-vivo measurements promise improvements by a more application-specific design, i.e. the additional current supply during CB underlies certain limitations in height and time, since both may increases the sensitivity for unwanted action potential excitation according to the strength-duration relationship [2].

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"Thank You."

A. Appendix

A.1. Complementary Calculations

The stability of the positive feedback loop of the circuit in Fig. 4.6 is to be examined by small signal analysis for low frequencies ($\omega \to 0$). Therefore, the overall feedback loop is opened at the gate of transistor M_3 to find the loop gain equation, which must hold the stability criteria for positive feedback loops

$$A_{LG} = |A(j\omega = 0) \cdot S(j\omega = 0) \cdot (C(j\omega = 0) - 1)| < 1\,, \tag{A.1}$$

where $A(j\omega = 0)$ is the DC voltage gain of the OPA, $S(j\omega = 0)$ of M_3 that is implemented as a source follower, and $C(j\omega = 0)$ of the basic current mirror components M_1 and M_2. For the sake of completeness of sec. 4.3.1 an expression for the source follower gain

$$S(j\omega = 0) = \frac{v_{D1}}{v_{G3}} \tag{A.2}$$

is derived. The abbreviations and symbols used refer to Fig. 4.6. First, the current through R_o is set equal to the current though transistor M_3

$$\frac{-v_G}{R_o} = g_{m3} \cdot (v_{G3} - v_{D1}) + \frac{v_G - v_{D1}}{r_{ds3}}\,. \tag{A.3}$$

Second, Eq. (4.7) is solved for

$$v_G = \frac{-v_{D1}}{r_{ds1} \cdot (g_{m1} + \frac{1}{R_o})}\,. \tag{A.4}$$

and substituted into Eq. (A.3), which finally yields to

$$S(j\omega = 0) = \frac{g_{m3} \cdot r_{ds3} \cdot R_o \cdot r_{ds1} \cdot (g_{m1} + \frac{1}{R_o})}{R_o + r_{ds3} + (1 + g_{m3} \cdot r_{ds3}) \cdot R_o \cdot r_{ds1} \cdot (g_{m1} + \frac{1}{R_o})} \tag{A.5}$$

$$= \frac{g_{m3} \cdot r_{ds3}}{\frac{R_o + r_{ds3}}{R_o \cdot r_{ds1} \cdot (g_{m1} + \frac{1}{R_o})} + (1 + g_{m3} \cdot r_{ds3})} = \frac{g_{m3} \cdot r_{ds3}}{\frac{1 + \frac{r_{ds3}}{R_o}}{g_{m1} \cdot r_{ds1} + \frac{r_{ds1}}{R_o}} + 1 + g_{m3} \cdot r_{ds3}}\,. \tag{A.6}$$

Assuming that $R_o >> r_{dsi}$, $S(j\omega = 0)$ can be simplified to

$$S(j\omega = 0) = \frac{1}{\frac{\frac{1}{g_{m1} \cdot r_{ds1}} + 1}{g_{m3} \cdot r_{ds3}} + 1} \lesssim 1\,. \tag{A.7}$$

A.2. FPGA Usage for Measurements

An external FPGA board from the company Opal Kelly is used for system measurement of the chip shown in Fig. 5.13, and for Twin-Track measurements as shown in Fig. 7.2. The FPGA controls the timing of the biphasic stimulator front-end and the charge balancers. Further it is used to program the stimulation parameters, as well as the controller settings of the PI-controlled OC. The description language VHDL was used for hardware implementation. Further, a graphical user interface (GUI) was developed using the programming language Python. An existing VHDL and Python program code of a former colleague Hagen Graf was adjusted and extended by the author for the needs of this work. The GUI communicates with the Opal Kelly board via an USB interface. Using the Opal Kelly environment, the data is first sent to an on-board microcontroller, which then communicates with the FPGA in the background.

The GUI is shown in Fig. A.1. In the upper left section, the FPGA is configured and started. In the upper right 'Inport/Export' section, an already exciting input file for all bit settings can be reloaded or a newly created file can be saved. In the section 'Pulse Generation', the stimulation and charge balancing events are timed. Within one stimulation period two values can be defined for each switch, which are time delay ('td') and pulse width ('tpw'). 'Anode' and 'Cathode' control switch $S_{a,c}$, respectively. 'En_active' controls S_{OC} to start and stop the integration of the PI-controlled OC, and with 'En_cap' the switch S_r can be activated to reset the integration cap. 'En_passive' is added to either control the on-chip integrated HV switch for passive charge balancing, or can be used in a Twin-Track measurement setup to control S_{IPCC} by changing an on-PCB connection. The 'Run Time' can be chosen either by seconds, or alternatively by a certain amount of repetitions of the stimulation period. The lower part, 'LV and HV Control Signals', is programmed to configure the bits for the stimulation parameters, offset adjustments and charge balancing settings. The configured bits are then sent via a scan chain in section 'Scan Chain Control'. As a verification, the scan length can be defined and feedback is given by changing the color of a label from orange ('Verification pending...') to green ('Verification successful').

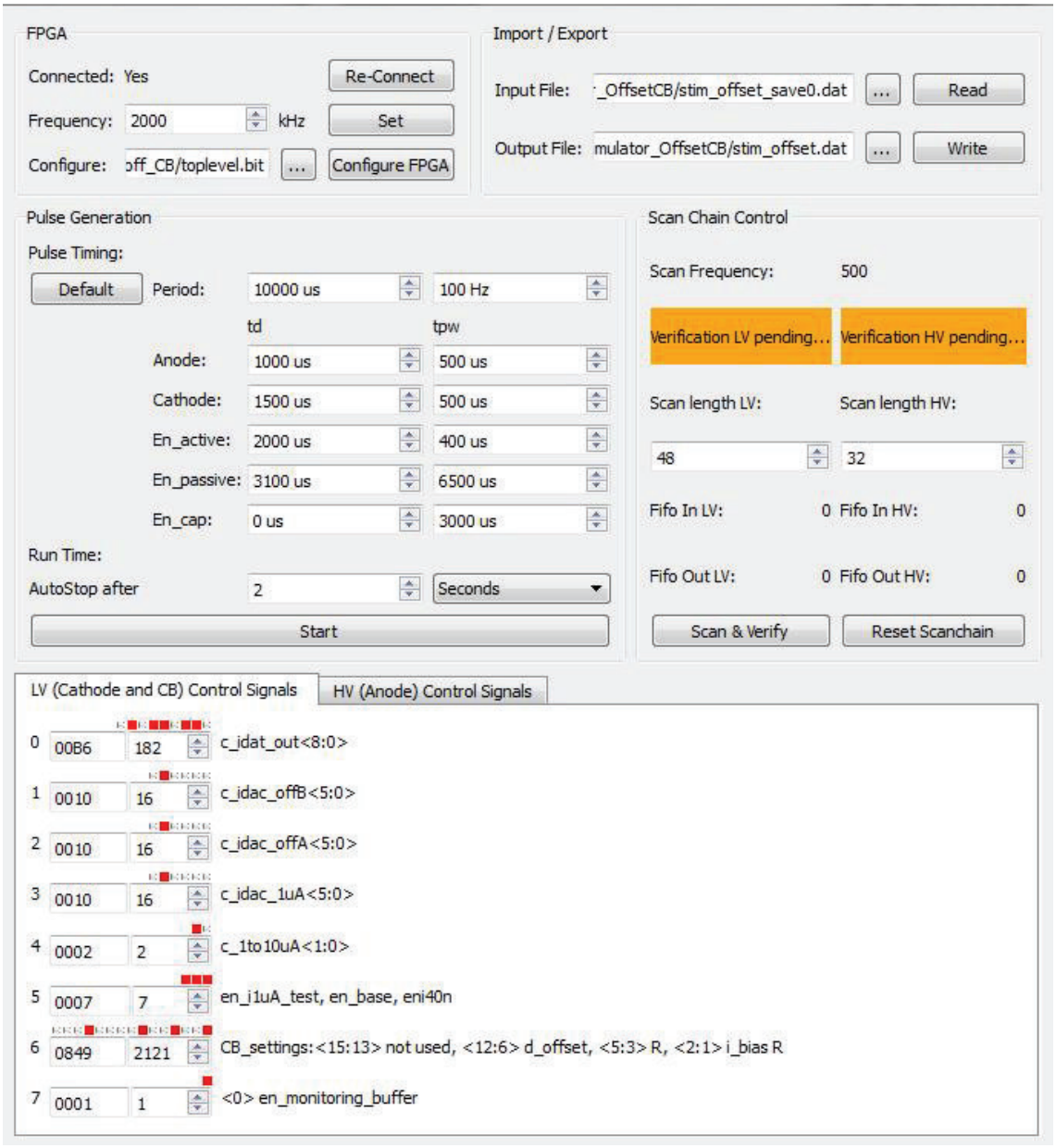

Figure A.1.: GUI of the FPGA used for PI-controlled OC and Twin-Track measurements.

B. Author's Scientific Track

B.1. Publications and Presentations

N. Butz, U. Kalita and Y. Manoli, "Active Charge Balancer With Adaptive 3.3 V to 38 V Supply Compliance for Neural Stimulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2021, doi: 10.1109/TCSI.2021.3101550.

A. Taschwer, **N. Butz**, M. Köhler, D. Rossbach, Y. Manoli, "Low-Power Neurostimulator ASIC mit frei konfigurierbarer Pulsform," in *Proc. Mikrosystemtechnik Kongress*, Oct 2019, pp. 213-214.

A. Taschwer, **N. Butz**, M. Köhler, D. Rossbach, and Y. Manoli, "A Charge Balanced Neural Stimulator with 3.3 V to 49 V Supply Compliance and Arbitrary Programmable Current Pulse Shapes," in *Proc. IEEE Biomedical Circuits and Systems Conference*, Oct 2018, pp. 1-4.

N. Butz, A. Taschwer, S. Nessler, Y. Manoli, and M. Kuhl, "A 22 V compliant 56 µW twin-track active charge balancing enabling 100% charge compensation even in monophasic and 36% amplitude correction in biphasic neural stimulators," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 8, pp. 2298-2310, Aug 2018.

N. Butz, U. Kalita, M. Kuhl, and Y. Manoli, "Active Charge Balancer with 6.6 V to 40 V Quad-Rail Power Supply Compliance for Neural Stimulators," in *Proc. IEEE International Symposium on Circuits and Systems*, May 2018, pp. 1-4.

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N. Butz, M. Kuhl, and Y. Manoli, "Intra-Pulse Charge Control,"

EP 3 100 766 B1, Dec 27, 2017

US 10,166,399 B2, Jan 1, 2019

Continuation-in-part: US 2019/0111249 A1, Apr 18, 2019

B.3. Supervised Thesis

Utpal Kalita, "Design of a CMOS Integrated Active Charge Balancer with Adaptive Power Supply Compliance for Neural Applications," Master's Thesis, July 2016.

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Nomenclature

Abbreviations	Denotation
AC/DC	alternating current/ direct current
ASIC	application specific integrated circuit
ATP	adenosine triphosphate
AP	action potential
BC	before Christ
C	capacitor
CB	charge balancing
CL	chloride
CM	common mode
CMFB	common mode feedback
CMOS	complementary MOS
CNS	central nervous system
D_i	diode i
DAC	digital-to-analog converter
DBS	deep brain stimulation
DDA	differential difference amplifier
DNL	differential nonlinearity
FDOTA	fully differential operational transconductance amplifier
FES	functional electric stimulation
FNS	functional neural stimulation
FPGA	field programmable gate array
FNS	Functional neural stimulation
FPGA	field programmable gate array
GM	transconductance
GmbH	Gesellschaft mit beschränkter Haftung
GUI	graphical user interface
H	hydrogen
H2O	water
HC	high-current
HF	high-frequency
HV	high-voltage
I	current
IC	integrated circuit
$I_{DAC,a,c}$	anodic and cathodic current DAC
IEEE	Institute of Electrical and Electronics Engineers

Abbreviations	Denotation
ILT	intermediate level translator
IMTEK	Institut für Mikrosystemtechnik (Department of Microsystems Engineering)
INL	integral nonlinearity
IPCC	Inter-Pulse Charge Control
IPCC-22 V	IPCC with a fixed 22 V supply
IPCC-AS	IPCC with an adaptive supply
Ir	iridium
IrO2	iridium oxide
K	potassium
LSB	least-significant-bit
LV	low-voltage
MC	Monte Carlo
MOS	metal oxide semiconductor
M_i	MOS transistor i
M_{sw}	switched transistor
Na	sodium
N_i	node i
NMOS	N-channel MOS
NS	nervous system
OC	Offset Compensation
OPA	operational amplifier
OTA_i	operational transconductance amplifier i
PCB	printed circuit board
PI	proportional-integral
P_i	PMOS terminal i
PM	phase margin
PMOS	P-channel MOS
PNS	peripheral nervous system
PSP	post synaptic potential
Pt	platinum
PT	proportional-lag
R	resistor
REF	reference
RF	radio frequency
Rg	range
RHP	high ohmic polysilicon resistor
$S_{a,c}$	switch for anodic and cathodic stimulus
S_{CB}	switch for charge balancing
S_i	switch i
S_{IPCC}	switch of IPCC
S_{OC}	switch of OC

Abbreviations	**Denotation**
S_P	switch for passive CB
S_r	switch for resting C_{int}
SRAM	static random-access memory
Stim	stimulation
T_{en}	enabling transistor
T_i	transistor with i
$T_{in,\ out}$	input and output terminal
UGBW	unity gain band width
VNS	vagus nerve stimulation
wc	worst case

Symbols	**Denotation**
a	area
A	gain
A_{CLG}	closed loop gain
A_{dc}	DC gain
A_{LG}	loop gain
$A(j\omega)$	transfer function of the OPA gain
A_O	open loop gain
$b_{Rsd,\ Rlin}$	LV control signals of R_{sd} and R_{lin}
β_i	transistor gain factor times W/L of transistor i
β_0	transistor gain factor
$C(j\omega)$	transfer function of the current mirror gain
C_{block}	blocking capacitance
C_C	Miller compensation capacitance
C_{gd}	gate drain capacitance
C_H	Helmholtz double layer capacitance
C_i	capacitance i
C_{int}	integration capacitance
C_Z	dominant capacitance of the zero
d_H	thickness of the Helmholtz double layer
ΔV_{GS}	gate-source voltage to open HV switch
ΔV_{LV}	LV quad-rail domain
ΔV_{safe}	safety window
en_i	enable signal i
ε	loop error
ε_0	electric constant
ε_r	elative permittivity of electrolyte
f	frequency
g_m	transconductance
G_m	overall transconductance
$g_{m,in}$	input transconductance

Symbols	Denotation
$G_{\mathrm{m}}(s)$	Laplace transform of the current driver
$G_{\mathrm{m,FDOTA}}$	overall transconductance of the FDOTA
G_{SD0}	output conductance at zero source-drain voltage
I_{mismatch}	mismatch current
$I(s)$	Laplace transform of the I controller
I_0	current intensity
I_{i}	current of branch i
$I_{\mathrm{a,c}}$	anodic and cathodic current amplitude
I_{bias}	biasing current
I_{CB}	charge balancing current in general
I_{D}	drain current
I_{E}	electrode current
I_{int}	integration current
I_{IPCC}	compensation current of IPCC
I_{OC}	output current of PI-controlled OC
I_{ref}	reference current
I_{rh}	rheobase current
I_{SS}	tail current
I_{Stim}	stimulus current
I_{th}	threshold current
k	scaling factor
k_{loop}	feedback factor
n	subthreshold slope factor
$P(s)$	Laplace transform of the P controller
p_{CM}	pole of current mirror
p_{E}	pole of electrode
p_{PI}	pole of PI-control
$PI(s)$	Laplace transform of the PI controller
P_{stat}	static power consumption
p_{OPA}	pole of OPA
p_{out}	output pole
Φ_{i}	switching signal i
Q	charge
$Q_{\mathrm{a,c}}$	anodic and cathodic charge
R_0	output resistance
R_{CMOS}	pseudo back-to-back CMOS resistance
R_{deg}	degeneration resistance
r_{dsi}	small signal resistance of transistor i
R_{F}	resistance modeling Faradic currents
R_{i}	resistance i
R_{lin}	resistance achieved by entering the linear region
r_{out}	output resistance

Symbols	Denotation
R_{on}	on-resistance of a switch
R_{S}	solution spreading resistance
R_{SD}	source-drain resistance
R_{sd}	resistance achieved by source degeneration
s	Laplace operator
$S(j\omega)$	transfer function of the source follower gain
$\mathrm{sw}_{50\mathrm{m}}$	switching signal to change from $\pm 100\,\mathrm{mV}$ to $\pm 50\,\mathrm{mV}$ safety window
σ	standard deviation
$\sum \mathrm{V}_{\mathrm{HV}}$	HV environment
t	time
t_{c}	chronaxie time
t_{d}	delay time
t_{dis}	discharge time
t_{w}	pulse width
$t_{\mathrm{wa,wc}}$	anodic and cathodic pulse width
τ	time constant
τ_{dis}	discharging time constant
V_{bias}	constant biasing voltage
V_{Cb}	voltage across C_{block}
V_{CH}	voltage across C_{H}
V_{CM}	body's quiescent potential
$V_{\mathrm{CM\_DET}}$	detected actual common mode voltage
$V_{\mathrm{CM\_LV}}$	LV output CM voltage of 1.65 V
V_{CMFB}	CMFB voltage
$V_{\mathrm{DD\_LV,\ DD\_HV}}$	upper supply rails
V_{di}	differential input voltage
V_{E}	electrode voltage
$V_{\mathrm{G,B,S,D}}$	gate, bulk, source, drain voltage
V_{head}	voltage headroom
$V_{\mathrm{HV+,HV-}}$	HV differential output voltages of the FDOTA
V_{i}	voltage i
V_{in}	input voltage
v_{in}	small signal input voltage
V_{int}	integrated voltage
$V_{\mathrm{LV+,LV-}}$	LV differential output voltages of the FDOTA
V_{out}	output voltage
v_{out}	small signal output voltage
V_{safe}	safety limit
$V_{\mathrm{SS,SS\_HV}}$	lower supply rails
V_{Stim}	stimulator output voltage
V_{T}	thermal voltage

Symbols	Denotation
V_{th}	threshold voltage
W/L	ratio of transistor dimensions width/length
ω	angular frequency
Z_{E}	complex impedance of electrode-tissue interface
$Z_{\mathrm{E}}(s)$	Laplace transform of Z_{E}
z_{E}	zero of electrode
z_{PI}	zero of PI-control